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Seventeen-Level Inverter Formed by Cascading Flying Capacitor and Floating Capacitor H-Bridges

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Abstract

A three-level flying capacitor inverter and cascaded H-bridge modules with float in capacitors have been proposed to generate 17 voltage levels. The current study discusses several features of the suggested inverter, such as capacitor voltage balancing. The simulation results are presented in order to investigate the performance of the suggested converter. The capacitor balancing algorithm's stability has been demonstrated during both transient and steady-state operation. Using one of the pole voltage combinations, all of the capacitors in this circuit can be instantly balanced. Another feature of this design is its ability to generate all voltages from a single dc-link power supply, allowing for back-to-back converter operation. Furthermore, the proposed inverter is capable of operating at all load power factors and modulation indices. Another benefit is that if one of the H-bridges fails, the inverter can still work at full load with a decreased number of levels. The dv/dt and common-mode voltage variations in this setup are quite minimal.

Key words: multilevel inverters, dc-link capacitor, PWM, space vector PWM

I. INTRODUCTION

The performance of medium and high-voltage drives has altered dramatically since the introduction of multilayer inverters [1–3]. As the number of voltage levels grows, the output voltage approaches a sine wave with less harmonic content, considerably boosting the drive's performance, as seen in [4] and [5]. The neutral point clamped inverter [6] is a pioneering development in the field of multilayer inverters. In contrast, [7] described the use of numerous isolated dc sources using H-bridges for plasma stabilization, creating different voltage levels. The work described in [8] evaluates the challenges with the cascading multiple rectifiers scheme and presents a solution for capacitor balancing. By altering the load current through capacitors, the work provided in [9] generates different voltage levels. In this case, the voltage through the capacitors can be kept constant by changing the direction of the load current through the capacitor by selecting redundant states with the same pole voltage. The notions offered in [10] are combined with those in [9] and [7]. The floating capacitor H-bridges are employed to generate different output voltages in this case. The capacitor voltages are kept at their proper values by cycling between redundant states for the same voltage level. The papers presented in [11–15] cover various aspects of using cascaded H-bridges and propose several efficient control techniques. Another type of multilevel converter that can be utilised for motor drive applications is modular multilevel converters, which are particularly popular in HVDC applications, as shown in [16]-[18].[19] presents the notion of a cascading flying capacitor inverter with a neutral point clamped inverter. ABB ACS 2000 is a commercial version of a similar concept [20]. Presents the idea of extending the number of levels by employing a flying capacitor inverter with cross-connected capacitors [21]. Presents an intriguing arrangement for generating 17 voltage levels utilising several capacitors. However, the capacitor voltages in [20] and [21] cannot be balanced instantly. Only at the fundamental frequency can they be balanced [22]. Presents a single-phase seventeen-level inverter setup that employs a high number of There is a power source as well as a floating load. This is more appropriate for STATCOM applications [23]. Describes an interesting algorithm for operating a seventeen-level inverter. In this paper, we propose a new 17-level inverter built by cascading three-level flying capacitor inverters with floating capacitor H-bridges that employs a single dc source and extracts all required voltage levels from it. The performance of the proposed configuration is experimentally validated for both steady-state and transient operation, and the results are provided.

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II POWER CIRCUIT TOPOLOGY

Now a day's many industrial applications have begun to require high power. Some appliances in the industries, however, require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi-level inverter has been introduced since 1975 as an alternative in high power and medium voltage situations. The Multilevel inverter is like an inverter and it is used for industrial applications as an alternative in high power and medium voltage situations.

One of the basic and well-known topologies among all multilevel inverters is Cascaded H-Bridge Multilevel Inverter. It can be used for both single and three phase conversion. It uses H-Bridge including switches and diodes.At least three voltage levels are required for a multilevel inverter. This can be accomplished by a single H-Bridge unit in Cascaded H-Bridge Multilevel Inverter. To keep the discussion snappy and clear I will go with the major points of this topology and also its advantages and disadvantages compared to other topologies.

A. PROPOSED CONVERTER

The proposed converter is a hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges. The three-phase power schematic is shown in Fig. 1. The voltages of capacitors AC1, BC1, and CC1 are maintained at Vdc/2. Capacitors AC2, BC2, and CC2 are maintained at voltage level of Vdc/4. Similarly capacitors AC3, BC3, and CC3 are maintained at voltage level of Vdc/8 and capacitors AC4, BC4, and CC4 are maintained at voltage level of Vdc/16. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by its previous stage. In addition to that, the CHBs can also be bypassed.

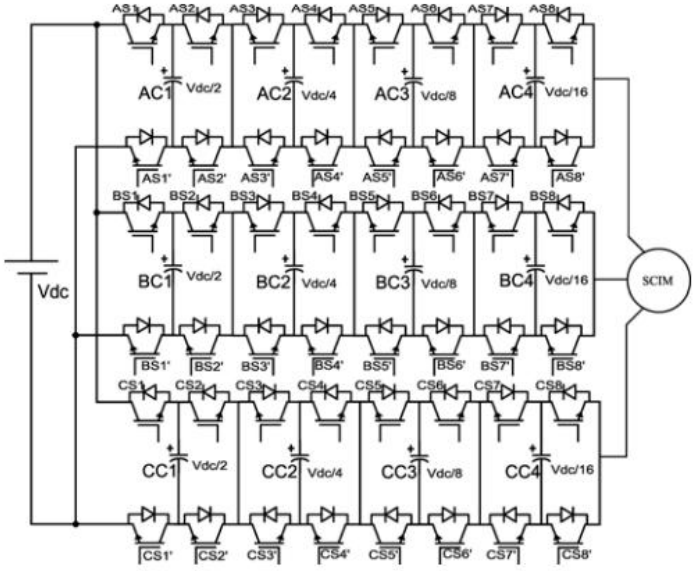

Fig. 1 Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

The resulting inverter pole voltage is the arithmetic sum of voltages of each stage. The schematic diagram for one phase of the proposed converter is shown in Fig. 2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in complementary fashion with appropriate dead time. Each switch pair has two distinct logic states, namely top device is ON (denoted by 1) or the bottom device is ON (denoted by 0).

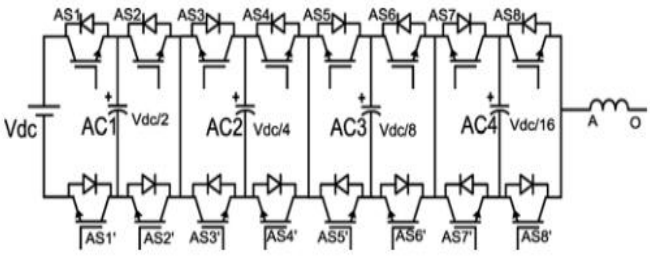

Fig. 2 One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

Therefore, there are 256 (28) distinct switching combinations possible. Each voltage level can be generated using one or more switching states (pole voltage redundancies). By switching through the redundant switching combinations (for the same pole voltage), the current through capacitors can be reversed and their voltages can be controlled to their prescribed values.

III SPACE VECTOR CONTROL REGION

A. PULSE-WIDTH MODULATION

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Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load. Along with maximum power point tracking (MPPT), it is one of the primary methods of reducing the output of solar panels to that which can be utilized by a battery. PWM is particularly suited for running inertial loads such as motors, which are not as easily affected by this discrete switching, because their inertia causes them to react slowly. The PWM switching frequency has to be high enough not to affect the load, which is to say that the resultant waveform perceived by the load must be as smooth as possible.

The rate (or frequency) at which the power supply must switch can vary greatly depending on load and application. For example, switching has to be done several times a minute in an electric stove; 100 or 120 Hz (double of the utility frequency) in a lamp dimmer; between a few kilohertz (kHz) and tens of kHz for a motor drive; and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies. The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle. PWM has also been used in certain communication systems where its duty cycle has been used to convey information over a communications channel.

In electronics, many modern microcontrollers (MCUs) integrate PWM controllers exposed to external pins as peripheral devices under firmware control by means of internal programming interfaces. These are commonly used for direct current (DC) motor control in robotics and other applications.

B. VOLTAGE REGULATION

PWM is also used in efficient voltage regulators. By switching voltage to the load with the appropriate duty cycle, the output will approximate a voltage at the desired level. The switching noise is usually filtered with an inductor and a capacitor. One method measures the output voltage. When it is lower than the desired voltage, it turns on the switch. When the output voltage is above the desired voltage, it turns off the switch. Each pole of the three-phase inverter can generate one of the 17 discrete pole voltage levels namely 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. For the proposed three-phase inverter, there is a total of 4913 (173) pole voltage combinations. Each pole voltage combination generates a voltage space vector V SV as given in the following equation:

$$\boldsymbol{V_{SV}} = V_{AN} + V_{BN}\angle 120^{\circ} + V_{CN}\angle 240^{\circ} \qquad (1)$$

Where VAN, VBN and VC N are the three-phase voltages

TABLE- I

Pole Voltage Redundancies and Capacitor States for Various Switching Combinations When Pole Sources Current

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S. No.	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª	S.No	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª
1	0	(0, 0, 0, 0, 0, 0, 0, 0)	0	0	0	0	42	Vdc/2	(1, 0, 0, 0, 0, 0, 0, 0)	+	0	0	0
2	Vdc/16	(0, 0, 0, 0, 0, 0, 0, 1)	0	0	0	−	43	9 Vdc/16	(0, 1, 0, 0, 0, 0, 0, 1)	−	0	0	−
3		(0, 0, 0, 0, 0, 1, 1, 0)	0	0	−	+	44		(0, 1, 0, 0, 0, 1, 1, 0)	−	0	−	+
4		(0, 0, 0, 1, 1, 0, 1, 0)	0	−	+	+	45		(0, 1, 0, 1, 1, 0, 1, 0)	−	−	+	+
5		(0, 1, 1, 0, 1, 0, 1, 0)	−	+	+	+	46		(1, 0, 0, 0, 0, 0, 0, 1)	+	0	0	−
6		(1, 0, 1, 0, 1, 0, 1, 0)	+	+	+	+	47		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	−	+
7	Vdc/8	(0, 0, 0, 0, 0, 1, 0, 0)	0	0	−	0	48		(1, 0, 0, 1, 1, 0, 1, 0)	+	−	+	+
8		(0, 0, 0, 1, 1, 0, 0, 0)	0	−	+	0	49		(1, 1, 1, 0, 1, 0, 1, 0)	0	+	+	+
9		(0, 1, 1, 0, 1, 0, 0, 0)	−	+	+	0	50	5 Vdc/8	(0, 1, 0, 0, 0, 1, 0, 0)	−	0	−	0
10		(1, 0, 1, 0, 1, 0, 0, 0)	+	+	+	0	51		(0, 1, 0, 1, 1, 0, 0, 0)	−	−	+	0
11	3 Vdc/16	(0, 0, 0, 0, 0, 1, 0, 1)	0	0	−	−	52		(1, 0, 0, 0, 0, 1, 0, 0)	+	0	−	0
12		(0, 0, 0, 1, 0, 0, 1, 0)	0	−	0	+	53		(1, 0, 0, 1,1, 0,0, 0)	+	−	+	0
13		(0, 0, 0, 1, 1, 0, 0, 1)	0	−	+	−	54		(1, 1, 1, 0, 1, 0, 0, 0)	0	+	+	0
14		(0, 1, 1, 0, 0, 0, 1, 0)	−	+	0	+	55	11 Vdc/16	(0, 1, 0, 0, 0, 1,0, 1)	−	0	−	−
15		(0, 1, 1, 0, 1, 0, 0, 1)	−	+	+	−	56		(0, 1, 0, 1, 0, 0, 1, 0)	−	−	0	+
16		(1, 0, 1, 0, 0, 0, 1, 0)	+	+	0	+	57		(0, 1, 0, 1, 1, 0, 0, 1)	−	−	+	−
17		(1, 0, 1, 0, 1, 0, 0, 1)	+	+	+	−	58		(1, 0, 0, 0, 0, 1, 0, 1)	+	0	−	−
18	Vdc/4	(0, 0, 0, 1, 0, 0, 0, 0)	0	−	0	0	59		(1, 0, 0, 1, 0, 0, 1, 0)	+	−	0	+
19		(0, 1, 1, 0, 0, 0, 0, 0)	−	+	0	0	60		(1, 0, 0, 1, 1, 0, 0, 1)	+	−	+	−
20		(1, 0, 1, 0, 0, 0, 0, 0)	+	+	0	0	61		(1, 1, 1, 0, 0, 0, 1, 0)	0	+	0	+
21	5 Vdc/16	(0, 0, 0, 1, 0, 0, 0, 1)	0	−	0	−	62		(1, 1, 1, 0, 1, 0, 0, 1)	0	+	+	−
22		(0, 0, 0, 1, 0, 1, 1, 0)	0	−	−	+	63	3 Vdc/4	(0, 1, 0, 1, 0, 0, 0, 0)	−	−	0	0
23		(0, 1, 0, 0, 1, 0, 1, 0)	−	0	+	+	64		(1, 0, 0, 1, 0, 0, 0, 0)	+	−	0	0
24		(0, 1, 1, 0, 0, 0, 0, 1)	−	+	0	−	65		(1, 1, 1, 0, 0, 0, 0, 0)	0	+	0	0
25		(0, 1, 1, 0, 0, 1, 1, 0)	−	+	−	+	66	13 Vdc/16	(0, 1, 0, 1, 0, 0, 0, 1)	−	−	0	−
26		(1, 0, 0, 0, 1, 0, 1, 0)	+	0	+	+	67		(0, 1, 0, 1, 0, 1, 1, 0)	−	−	−	+
27		(1, 0, 1, 0, 0, 0, 0, 1)	+	+	0	−	68		(1, 0, 0, 1, 0, 0, 0, 1)	+	−	0	−
28		(1, 0, 1, 0, 0, 1, 1, 0)	+	+	−	+	69		(1, 0, 0, 1, 0, 1, 1, 0)	+	−	−	+
29	3 Vdc/8	(0, 0, 0, 1, 0, 1, 0, 0)	0	−	−	0	70		(1, 1, 0, 0, 1, 0, 1, 0)	0	0	+	+
30		(0, 1, 0, 0, 1, 0, 0, 0)	−	0	+	0	71		(1, 1, 1, 0, 0, 0, 0, 1)	0	+	0	−
31		(0, 1, 1, 0, 0, 1, 0, 0)	−	+	−	0	72		(1, 1, 1, 0, 0, 1, 1, 0)	0	+	−	+
32		(1, 0, 0, 0, 1, 0, 0, 0)	+	0	+	0	73	7 Vdc/8	(0, 1, 0, 1, 0, 1, 0, 0)	−	−	−	0
33		(1, 0, 1, 0, 0, 1, 0, 0)	+	+	−	0	74		(1, 0, 0, 1, 0, 1, 0, 0)	+	−	−	0
34	7 Vdc/16	(0, 0, 0, 1, 0, 1, 0, 1)	0	−	−	−	75		(1, 1, 0, 0, 1, 0, 0, 0)	0	0	+	0
35		(0, 1, 0, 0, 0, 0, 1, 0)	−	0	0	+	76		(1, 1, 1, 0, 0, 1, 0, 0)	0	+	−	0
36		(0, 1, 0, 0, 1, 0, 0, 1)	−	0	+	−	77	15 Vdc/16	(0, 1, 0, 1, 0, 1, 0, 1)	−	−	−	−
37		(0, 1, 1, 0, 0, 1, 0, 1)	−	+	−	−	78		(1, 0, 0, 1, 0, 1, 0, 1)	+	−	−	−
38		(1, 0, 0, 0, 0, 0, 1, 0)	+	0	0	+	79		(1, 1, 0, 0, 0, 0, 1, 0)	0	0	0	+
39		(1, 0, 0, 0, 1, 0, 0, 1)	+	0	+	−	80		(1, 1, 0, 0, 1, 0, 0, 1)	0	0	+	−
40		(1, 0, 1, 0, 0, 1, 0, 1)	+	+	−	−	81		(1, 1, 1, 0, 0, 1, 0, 1)	0	+	−	−
41	Vdc/2	(0, 1, 0, 0, 0, 0, 0, 0)	−	0	0	0	82	Vdc	(1, 1, 0, 0, 0, 0, 0, 0)	0	0	0	0

These 4193 pole voltage combinations when marked on a space vector plane spread across 817 distinct space vector locations. Each of the 817 space vector locations can have more than one pole voltage combination (phase voltage redundancy) with different common mode voltages. In addition, each pole voltage can have one or more redundant switching combination (pole voltage redundancy which can be used to balance the capacitor voltages of that particular phase) as described in the previous section. The diagram of the space vector polygon formed by these

817 locations is shown in Fig. 3. There 16 concentric hexagons that form the space vector control region of the proposed seventeen-level inverter.

The space vectors on the outer hexagon do not have any phase voltage redundancies. The locations on the second largest hexagon have double redundancy and can be generated with two sets of pole voltages with different common mode voltages. For the smaller inner hexagons, the number of pole voltage combinations for generating the space vector locations increases. There are 16 redundant pole voltage combinations each with a different common mode voltage for each space vector location on the inner most hexagons. Therefore, the zero state at the center has a total of seventeen pole voltage combinations all of which generate zero differential mode voltage.

This method of balancing the capacitor voltages at all load currents and power factors instantaneously has been observed for 17 pole voltage levels. They are 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. However, by switching through all the possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle. There are 82 switching combinations (see Table I) that can be used to generate the above mentioned 17 pole voltage levels where instantaneous capacitor voltage balancing is possible. The effect of 82 switching combinations on every capacitor's charge state (charge or discharge) for positive direction of current (i.e., when the pole is sourcing current as marked in Fig. 3.2) is shown in Table I.

For negative direction of current, the effect of the switching state on the capacitor is reversed. For example, when the controller demands a pole voltage of Vdc/16, there are fi e different redundant switching combinations to generate it. Each switching combination has a different effect on the state of charge

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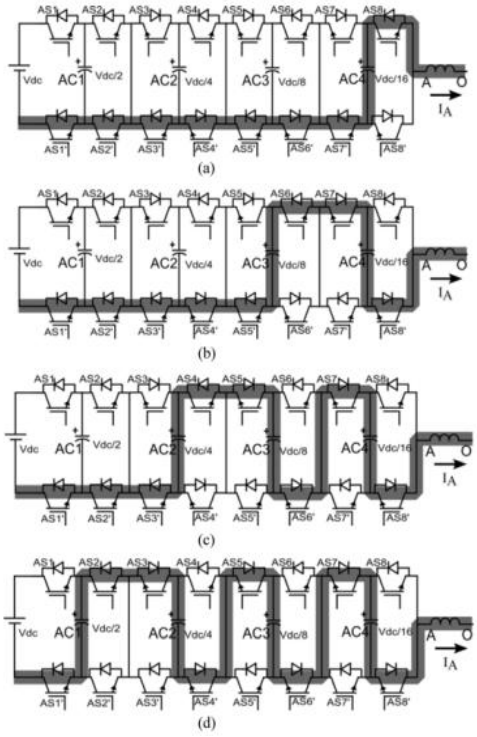
of the capacitors. When the switching state (0, 0, 0, 0, 0, 0, 0, 1) (see Table I) is applied, the capacitor C4 discharges when the pole is sourcing current as [see Fig. 3(a)]. To balance the capacitor C4 and to bring its voltage back to the prescribed value (Vdc/16), one of the other four switching combinations is applied Fig. 3.1(b)–(e). It can be observed that when switching state (0, 0, 0, 0, 0, 1, 1, 0) is applied, the direction of current in the capacitor C4 is reversed [see Fig. 3.(b)] and the capacitor C4 charges. However in this process, the capacitor C3 is discharged. If the capacitor C3 needs charging, switching state redundancy of (0, 0, 0, 1, 1, 0, 1, 0) is applied [see Fig. 3.(c)] which discharges C2.

To charge C2 one of the switching redundancies shown in Fig. 3.(d) and (e) is applied based on the state of charge of capacitor C1. If switching state (0, 1, 1, 0, 1, 0, 1, 0) is applied, the capacitor C1 is discharged and this state charges all the other capacitors as shown in Fig. 3.(d). Finally, when switching state of (1, 0, 1, 0, 1, 0, 1, 0) is applied, all the four capacitors are charged for positive direction of current as shown in Fig. 3.2(e). By switching through the redundant pole voltage combinations, it can be observed that the all the capacitors' voltages can be maintained at their prescribed values while generating pole voltage of Vdc/16 for positive direction of current. If all the capacitors need discharging, the capacitor C4 is discharged firs and the remaining capacitors can be discharged during subsequent switching cycles when C4 needs to be charged. For negative direction of current, the effect of the capacitor voltages is the opposite.



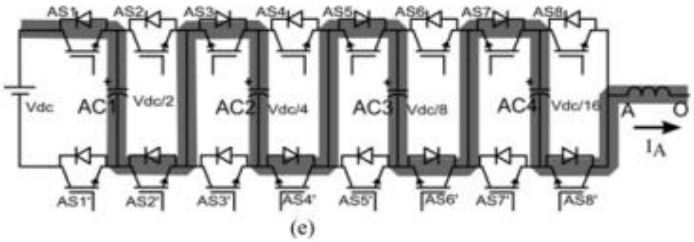


Fig. 3 Switching Redundancies for pole voltage of Vdc/16 (a) Current path for switching state (0, 0, 0, 0, 0, 0, 0, 1). (b) Current path for switching state (0, 0, 0, 0, 0, 1, 1, 0). (c) Current path for switching state (0, 0, 0, 1, 1, 0, 1, 0). (d) Current path for switching state (0, 1, 1, 0, 1, 0, 1, 0). (e) Current path for switching state (1, 0, 1, 0, 1, 0, 1, 0).

The entire process of capacitor voltage balancing for pole voltage of Vdc/16 that has been explained is illustrated in Fig. 3. Here, the capacitor voltage variation with application of various redundant states for pole voltage of Vdc/16 has been shown for positive direction of current. For other pole voltages namely, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc, a similar strategy can be used to balance all the capacitor voltages. The switching frequency of any CHB module is at most the PWM switching frequency of the converter. This is due to the synchronization of application of the switching state with every PWM transition (the switching state is latched till the next PWM transition). Moreover in this scheme, only the capacitors that contribute to the output pole voltages are switched.

IV SIMULATION RESULTS

For validating the operation at different scenarios, the system is simulated in MATLAB/Simulink and a hardware prototype is built in the laboratory.

A. SIMULATION MODEL

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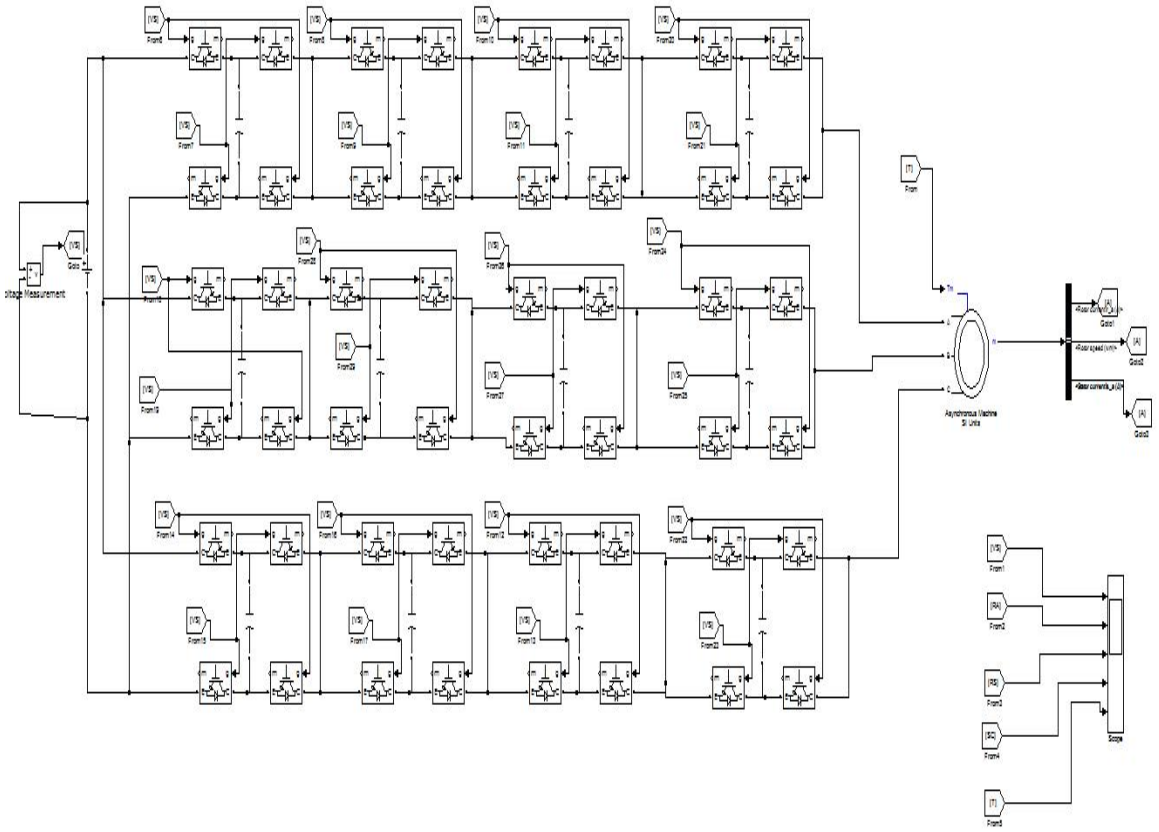

Fig. 4 Simulation model

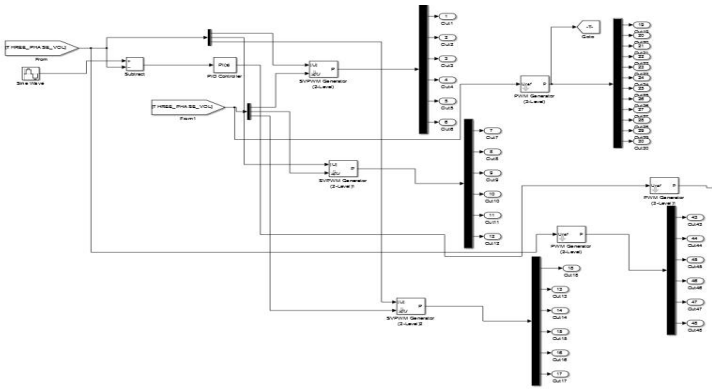

Fig. 5 SVPWM Control diagram

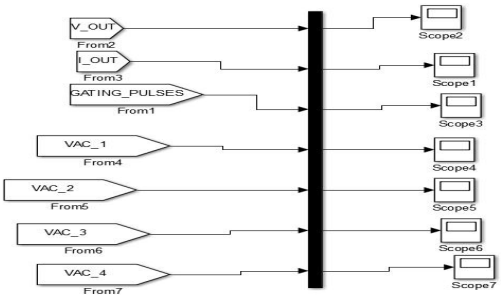

Fig. 6 Results

B. SIMULATION RESULTS

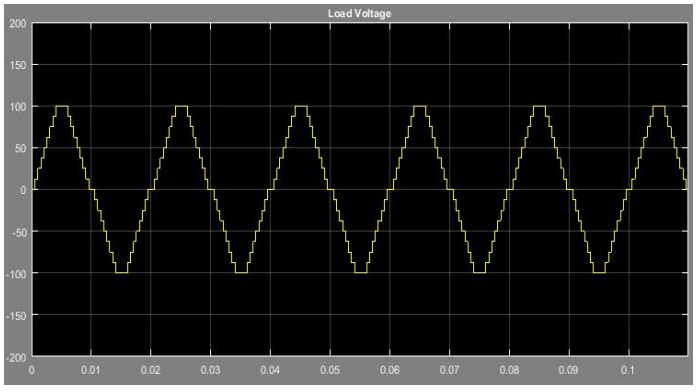

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Fig. 7 Output voltage

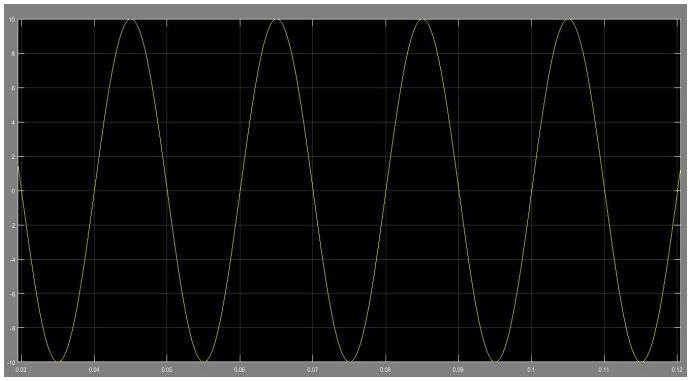
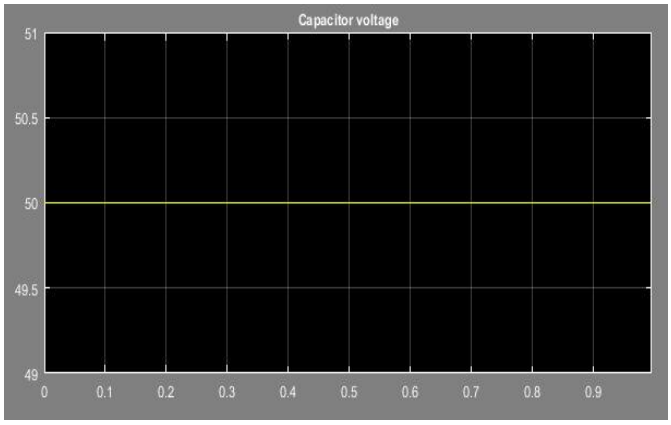
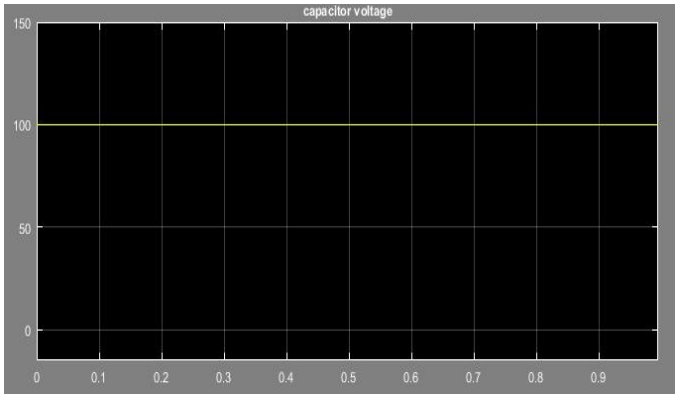


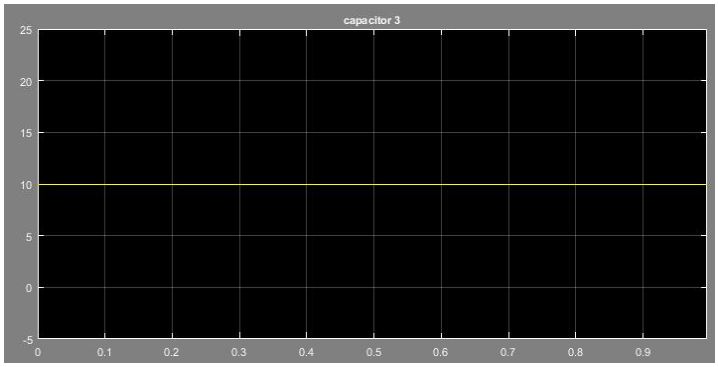
Fig. 8 Output current



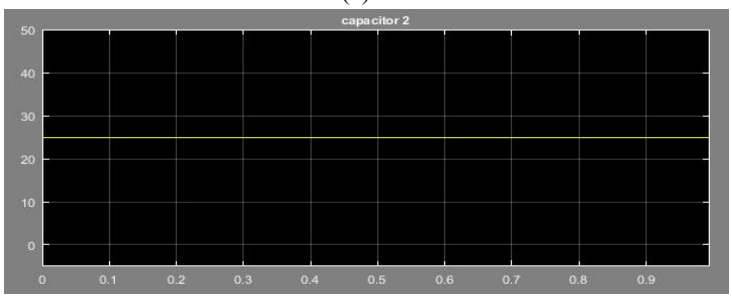
(a)



(b)



(c)



(d)

Fig. 8 Capacitor voltages

V. CONCLUSION

A new 17-level inverter configuration formed by cascading a three-level flying capacitor and three floating capacitor H-bridges has been proposed for the first time. The voltages of each of the capacitors are controlled instantaneously in few switching cycles at all loads and power factors obtaining high performance output voltages and currents. The proposed configuration uses a single dc link and derives the other voltage levels from it. This enables back-to-back converter operation where power can be drawn and supplied to the grid at prescribed power factor. Also, the proposed 17-level inverter has improved reliability. In case of failure of one of the H-bridges, the inverter can still be operated with reduced number of levels supplying full power to the load. This feature enables it to be used in critical applications like marine propulsion and traction where reliability is of highest concern. Another advantage of the proposed configuration is modularity and symmetry in structure which enables the inverter to be extended to more number of phases like e-phase and six-phase configuration with the same control scheme. The proposed inverter is analyzed and its performance is experimentally verified for various modulation indices and load currents by running a three-phase 3-kW squirrel cage induction motor.

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