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Closed loop control of Bidirectional Buck-Boost Converter in a Smart Grid using Photovoltaic and Energy Storage Systems

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ABSTRACT

—This paper proposes a new bidirectional buck-boost converter, which is a key component in a photovoltaic and energy storage system (PV-ESS). Conventional bidirectional buck-boost converters for ESSs operate in discontinuous conduction mode (DCM) to achieve zero-voltage-switching turn-on for switches. However, operation in DCM causes high ripples in the output voltage and current, as well as low power-conversion efficiency. To improve on the performance of the conventional converter, the proposed converter has a new combined structure of a cascaded buck-boost converter and an auxiliary capacitor. The combined structure of the proposed converter reduces the output current ripple by providing a current path and the efficiency is increased. A prototype was built and tested to verify the effectiveness of the converter. The proposed converter has a maximum efficiency of 98%, less than 5.14 Vp.p of output voltage ripple, and less than 7.12 Ap.p of output current ripple. These results were obtained at an input voltage of 160 V, switching frequency of 45 kHz, output voltage of 80 ~ 320 V, and output power of 16 ~ 160 W. The experimental results show that the proposed converter has improved performance compared to the conventional converter.

Index Terms—DC-DC power conversion, Energy storage, Pulse width modulated power converters.

I.INTRODUCTION

SMART grid (Fig. 1) is future electric energy system that has been studied to reduce mismatching between sources of electricity (such as renewable energy and power plants) and electricity consumers (homes, vehicles, factories, etc.). However, the energy production of renewable energy depends on environmental conditions. Therefore, an energy storage system (ESS) is needed in a smart grid to provide stability and efficiently manage the renewable energy [1-3].

An ESS consists of a battery that stores electric energy and a bidirectional DC-DC converter that transfers energy from battery and renewable energy source in both directions [4-9]. A conventional bidirectional DC-DC converter uses a half-bridge converter with two switches based on a buck or boost DC-DC converter.

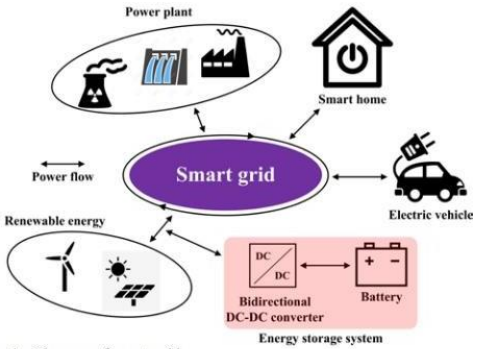

Fig. 1. Diagram of smart grid.

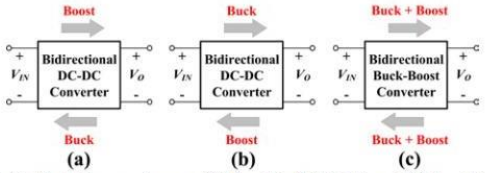

Fig. 2. Block diagrams in case of (a) $V_{IN} < V_O$, (b) $V_{IN} > V_O$, and (c) $V_{IN} < V_O$ & $V_{IN} > V_O$.

In the buck mode of the converter, electric energy is transferred from a high voltage (HV) port to the low voltage (LV) port. In boost mode, the electric energy is transferred from the LV port to the HV port. The conventional bidirectional converter has a limitation in that it can only be operated in buck mode in one direction and boost mode in the other direction (Fig. 2(a) and Fig. 2(b)) [10-12]. Therefore, when the input is a photovoltaic (PV) module and the output is battery cells in a smart grid, a half bridge converter based on a buck or boost converter cannot be used because of the following reasons: 1) The

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battery cells repeatedly perform charging and discharging operations, resulting in large voltage variation [13, 14]. 2) The PV module has a large voltage variation that depends on the module temperature and the solar irradiance [15-17]. Thus, the ranges of the input voltage and output voltage can overlap [18, 19]. Bidirectional buck-boost converters (Fig. 2(c)) were introduced for use in cases of overlapping input and output voltages [19-28]. They can operate in both buck and boost modes in both directions. A combined half-bridge (CHB) converter (Fig. 3(a)) is the most basic bidirectional buck-boost converter and has a symmetric structure with respect to the storage capacitor CS [20, 21]. There is one inductor at the input port and one at the output port, which results in low voltage ripples in the input and output. However, because the CHB converter uses two inductors of the same size, it is large and has a low power-conversion efficiency ηe due to the DC-offset current of each inductor. Cascaded buck-boost (CBB) converter (Fig. 3(b)), along with the CHB converter, has been commonly used in ESSs. Compared with the CHB converter, CBB converter is smaller and has higher ηe because it uses only one inductor L [19, 22-28]. Recently, research has been actively conducted on bidirectional buck-boost DC-DC converters in discontinuous conduction mode (DCM) because this mode can achieve zero-voltage-switching (ZVS) turn-on of the switches [19, 26-28]. However, operation in DCM increases the current ripple of L, which affects the output current ripple and increases. In this paper, an enhanced CBB converter is proposed to improve on the performance of the conventional CBB converter. The proposed converter is targeted to a PV-ESS system that uses a micro-inverter, which has been widely used in a smart grid [29, 30]. The converter has a new combined structure of a CBB converter and an auxiliary capacitor.

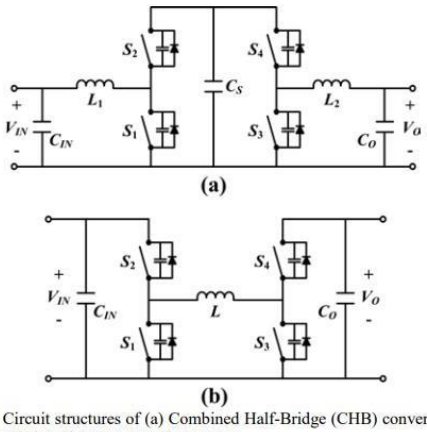

Fig. 3. Circuit structures of (a) Combined Half-Bridge (CHB) converter and (b) Cascaded Buck-Boost (CBB) converter.

This structure can reduce the output voltage ripple and increase ηe by effectively reducing the output current ripple. The circuit structure and operating principle of the proposed converter are described in Section II, and design considerations are given in Section III. Experimental results are given in Section IV, and a conclusion is given in Section V

II. PROPOSED DC-DC CONVERTER

A. Circuit Structure The proposed converter (Fig. 4) consists of a conventional CBB converter and an auxiliary capacitor (Ca), and has a symmetric structure with respect to Ca and L. The CBB converter consists of two capacitors (CIN, CO), four switches (S1, S2, S3, S4), and an inductor (L). Four switches (S1, S2, S3, S4) and an inductor (L) control the direction of energy transfer and the ratio between the input voltage and output voltage. Four switches are turned on in the ZVS condition by operating in DCM. Two capacitors (CIN, CO) reduce the output voltage ripple and noise, and an auxiliary capacitor (Ca) reduces the output current ripple by providing a current path.

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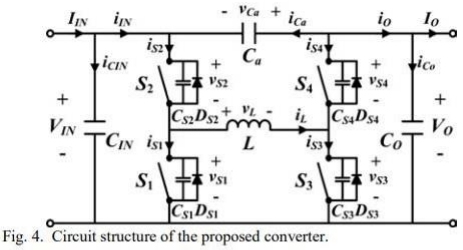

Fig. 4. Circuit structure of the proposed converter.

TABLE I
STATES OF SWITCHES IN SIX OPERATING CONDITIONS

Six operating conditions		Switches			
Directions of energy transfer	Types of the operation	S_1	S_2	S_3	S_4
$V_{IN} \rightarrow V_O$	Buck	1 - D	D	0	1
	Buck-Boost	1 - D	D	D	1 - D
	Boost	0	1	D	1 - D
$V_O \rightarrow V_{IN}$	Buck	0	1	D	1 - D
	Buck-Boost	1 - D	D	D	1 - D
	Boost	1 - D	D	0	1

B. **Principle of Operation:** The proposed converter operates with a fixed switching period TS and controls the voltage gain by changing the duty ratio D of the switches (S1, S2, S3, S4) from 0 to 1. Each switch has four states in six operating conditions created by the energy transfer directions between VIN and VO and the types of operation (buck, boost, andbuck-boost), as shown in Table I. Due to the symmetric structure with respect to Ca and L, the operations are separated by only the types of operation in one direction of energy transfer (VIN → VO). To simplify the analysis of the operation, the following assumptions are made: 1) the inductor and all capacitors are lossless, 2) the voltage ripples of CIN, Ca, and CO are small enough to assume that VIN, VCa, and VO are constant voltage sources, and 3) the converter operates in steady state. (1) Buck mode When the proposed converter operates in buck mode, it has four distinct operating modes (Mode 1 ~ 4). The equivalent circuits and operating waveforms are shown in Fig. 5 and Fig. 6. Mode 1 (Fig. 5(a), t0 ≤ t ≤ t1) starts when S2 is turned on. At t = t0, S2 achieves ZVS turn-on because the body diode DS2 of S2 is turned on before t = t0. Then, the voltage vL of L becomes VIN – VO, and the current iL of L is expressed as

$$i_L(t) = i_L(t_0) + \frac{V_{IN} - V_O}{L}(t - t_0). \quad (1)$$

The current i_{S2} of S_2 is equal to i_L, so i_{S2} is expressed as

$$i_{S2}(t) = i_L(t_0) + \frac{V_{IN} - V_O}{L}(t - t_0).$$

In this mode, the current i_{Ca} of C_a, the current i_{Co} of C_O, the output current i_O, and the load current I_O have the following relations: $i_O = i_{Co} + I_O$, $i_{Co} = i_{Ca} \cdot C_O/C_a$, and $i_O = i_L - i_{Ca}$. Therefore, i_{Ca} and i_O can be derived as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}[i_L(t) - I_O]$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (2)$$

The voltage v_{Ca} across the auxiliary capacitor C_a is expressed as

$$v_{Ca}(t) = V_{Ca} + \Delta v_{Ca,AC}(t)$$

where V_{Ca} and $\Delta v_{Ca,AC}$ represent the DC voltage and the AC ripple voltage across the C_a, respectively. Because $V_{Ca} >> \Delta v_{Ca,AC}$, v_{Ca} can be approximated as

$$v_{Ca}(t) \approx V_{Ca} = V_O - V_{IN}.$$

Mode 2 (Fig. 5(b), t1 ≤ t ≤ t2) starts when S2 is turned off. At this time, S1 remains in the off state to prevent a shoot-through problem with S1 and S2. In this mode, the output capacitor CS1 of S1 discharges from VIN to 0, and the output capacitor CS2 of S2 charges from 0 to VIN. Shortly after the discharging of CS1 and charging of CS2 are finished, the body diode DS1 of S1 is turned on. Mode 3 (Fig. 5(c), t2 ≤ t ≤ t3) starts with the ZVS turn-on of S1 because DS1 is turned on before t = t2. Then, vL becomes -VO, and thereby iL is expressed as.

$$i_L(t) = i_L(t_2) - \frac{V_O}{L}(t - t_2). \quad (3)$$

The current i_{S1} of S_1 is equal to $-i_L$, so i_{S1} is obtained as

$$i_{S1}(t) = -i_L(t_2) + \frac{V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}[i_L(t) - I_O] \quad (4)$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (5)$$

Mode 4 (Fig. 5(d), t3 ≤ t ≤ t4) starts when S1 is turned off and S2 remains in the off state. In this mode, CS1 charges from 0 to VIN, and CS2 discharges from VIN to 0. Shortly after the charging of CS1 and discharging of CS2 are finished, DS2 is turned on. At t = t0, iL has an initial value of iL(t0), and iL(t0) is obtained as

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follows: By inserting t = t2 into (1), the current ripple ΔiL of iL is obtained as ( ) ( ) S IN O LL L DT L VV titii − 02 =−=Δ , (6) where DTS = t2 – t0. The average current of L for one TS is obtained as = IO by applying the ampere-second balance law for capacitors to L ( ) ( ) ( ) Ca Co ++= Itititi O . Then, iL(t0) = - ΔiL/2 is represented as.

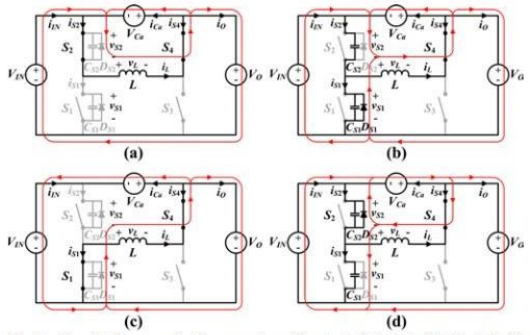

Fig. 5. Circuit diagrams for the operation of buck; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

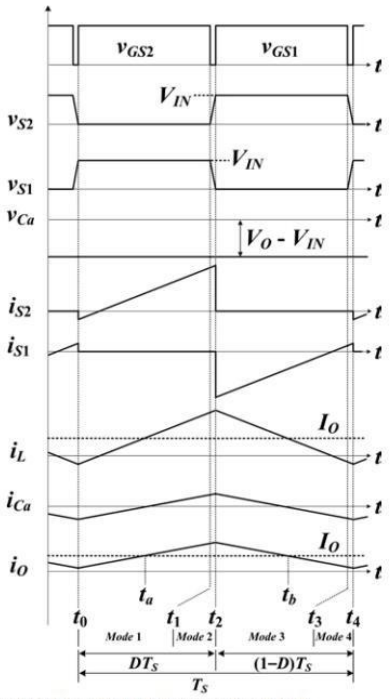

Fig. 6. Operational waveforms in the operation of buck.

$$i_L(t_0) = I_O - \frac{V_{IN} - V_O}{2L} DT_S, \quad (7)$$

and $i_L(t_2) = \langle i_L \rangle + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_O + \frac{V_{IN} - V_O}{2L} DT_S. \quad (8)$$

(2) Boost mode The boost operation also has four distinct operating modes (Mode 1 ~ 4), and the equivalent circuits and operating waveforms are shown in Fig. 7 and Fig. 8, respectively. Mode 1 (Fig. 7(a), t0 ≤ t ≤ t1) starts when S3 is turned on. At t = t0, S3 achieves ZVS turn-on because the body diode DS3 of S3 is turned on before t = t0. Then, vL becomes VIN, and iL is expressed as.

$$i_L(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0). \quad (9)$$

The current i_{S3} of S_3 is the same as i_L, so i_{S3} is expressed as

$$i_{S3}(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0).$$

Because $i_O = -i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = -\frac{C_a}{C_a + C_O} I_O$$

$$i_O(t) = \frac{C_a}{C_a + C_O} I_O. \quad (10)$$

The voltage v_{Ca} across the auxiliary capacitor C_a is expressed as

$$v_{Ca}(t) = V_{Ca} + \Delta v_{Ca,AC}(t).$$

Because $V_{Ca} >> \Delta v_{Ca,AC}$, this expression can be approximated as

$$v_{Ca}(t) \approx V_{Ca} = V_O - V_{IN}$$

Mode 2 (Fig. 7(b), t1 ≤ t ≤ t2) starts when S3 is turned off and S4 remains in the off state. In this mode, the output capacitor CS3 of S3 charges from 0 to VO, and the output capacitor CS4 of S4 discharges from VO to 0. Shortly after the charging of CS3 and discharging of CS4 are finished, the body diode DS4 of S4 is turned on. Mode 3 (Fig. 7(c), t2 ≤ t ≤ t3) starts with the ZVS turn-on of S4 because DS4 is turned on before t = t2. Then, vL becomes VIN - VO, and iL is expressed as.

$$i_L(t) = i_L(t_2) + \frac{V_{IN} - V_O}{L}(t - t_2). \quad (11)$$

The current i_{S4} of S_4 is equal to $-i_L$, so i_{S4} is obtained as

$$i_{S4}(t) = -i_L(t_2) - \frac{V_{IN} - V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}[i_L(t) - I_O] \quad (12)$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (13)$$

Mode 4 (Fig. 7(d), t3 ≤ t ≤ t4) starts when S4 is turned off and S3 remains in off-state. In this mode, CS3 discharges from VO to 0 and CS4 charges from 0 to VO. Shortly after the discharging of CS3 and charging of CS4 are finished, DS3 is turned on. By inserting t = t2 into (9), ΔiL for boost operation is obtained as.

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$$\Delta i_L = i_L(t_2) - i_L(t_0) = \frac{V_{IN}}{L} DT_S, \quad (14)$$

where $DT_S = t_2 - t_0$. Because $\langle i_L \rangle = I_{IN}$ and $i_L(t_0) = \langle i_L \rangle - \Delta i_L/2$, $i_L(t_0)$ is expressed as

$$i_L(t_0) = I_{IN} - \frac{V_{IN}}{2L} DT_S. \quad (15)$$

$i_L(t_2) = \langle i_L \rangle + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_{IN} + \frac{V_{IN}}{2L} DT_S. \quad (16)$$

(3) Buck-boost mode The buck-boost operation has four distinct operating modes (Mode 1 ~ 4), and the equivalent circuits and operating waveforms are shown in Fig. 9 and Fig. 10, respectively. Mode 1 (Fig. 9(a), t0 ≤ t ≤ t1) starts when S2 and S3 are turned on. At t = t0, S2 and S3 achieve ZVS turn-on because DS2 and DS3 are turned on before t = t0. Then, vL becomes VIN, and iL is expressed as.

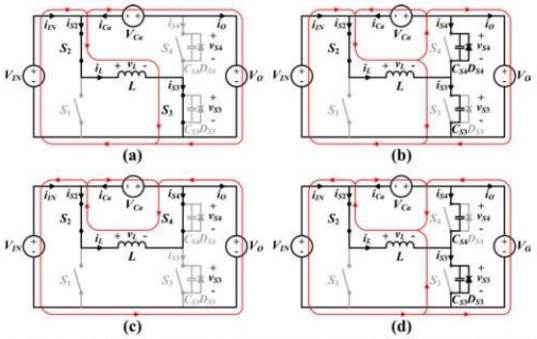

Fig. 7. Circuit diagrams for the operation of boost; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

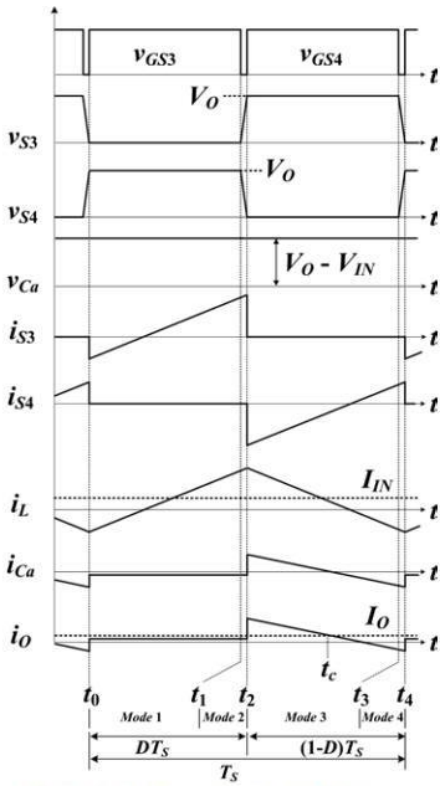

Fig. 8. Operational waveforms in the operation of boost.

$$i_L(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0). \quad (17)$$

Both i_{S2} and i_{S3} are same as i_L, so they are expressed as

$$i_{S2}(t) = i_{S3}(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0).$$

Because iO = -iCa, iO = iCo + IO, and iCo = iCa ·CO/Ca, iCa and iO are expressed as.

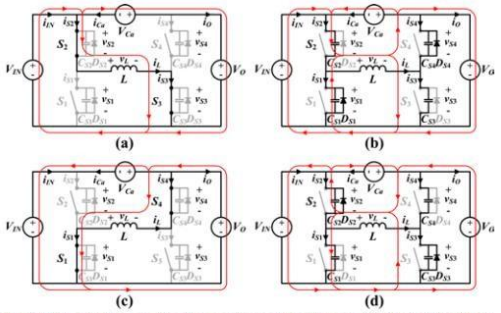

Fig. 9. Circuit diagrams for the operation of buck-boost; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

$$i_{Ca}(t) = -\frac{C_a}{C_a + C_O} I_O \quad (18)$$

$$i_O(t) = \frac{C_a}{C_a + C_O} I_O. \quad (19)$$

$v_{Ca}(t)$ is obtained using the equation (18) as

$$v_{Ca}(t) = v_{Ca}(t_0) + \frac{1}{C_a}\int_{t_0}^{t} i_{Ca}(t)dt \approx v_{Ca} + \frac{1}{C_a}\left[\frac{-C_a I_O}{C_a + C_O}(t - t_0)\right]$$

$$= V_O - V_{IN} - \frac{I_O}{C_a + C_O}(t - t_0).$$

Mode 2 (Fig. 9(b), t1 ≤ t ≤ t2) starts when S2 and S3 are turned off and S1 and S4 remain in the off state. In this mode, CS2 and CS3

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charge from 0 to VIN and from 0 to VO, respectively. CS1 and CS4 discharge from VIN to 0 and from VO to 0, respectively. Shortly after the charging and discharging processes are finished, the DS1 and DS4 are turned on. Mode 3 (Fig. 9(c), t2 ≤ t ≤ t3) starts with the ZVS turn-on of S1 and S4 because DS1 and DS4 are turned on before t = t2. Then, vL becomes -VO, and iL is expressed as.

$$i_L(t) = i_L(t_2) - \frac{v_O}{L}(t - t_2). \quad (20)$$

i_{S1} and i_{S4} are equal to $-i_L$, so they are obtained as

$$i_{S1}(t) = i_{S4}(t) = -i_L(t_2) + \frac{V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}[i_L(t) - I_O] \quad (21)$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (22)$$

v_{Ca} is obtained using equations (20) and (21) as

$$v_{Ca}(t) = \frac{1}{C_a}\int_{t_2}^{t} i_{Ca}(t)dt + v_{Ca}(t_2)$$

$$= \frac{1}{C_a + C_O}\left[(i_L(t_2) - I_O)(t - t_2) - \frac{V_O}{2L}(t - t_2)^2\right] + v_{Ca}(t_2).$$

Mode 4 (Fig. 9(d), t3 ≤ t ≤ t4) starts when S1 and S4 are turned off and S2 and S3 remain in the off state. In this mode, CS2 and CS3 discharge from VIN to 0 and from VO to 0, respectively. CS1 and CS4 charge from 0 to VIN and from 0 to VO, respectively. Shortly after the discharging and charging processes are finished, DS2 and DS3 are turned on. By inserting t = t2 into (17), ΔiL is obtained for buck-boost operation as.

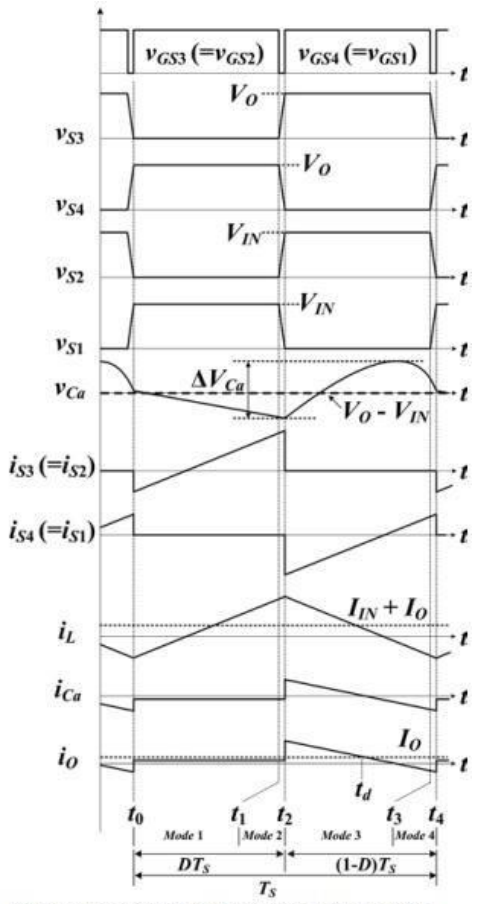


Fig. 10. Operational waveforms in the operation of buck-boost.

By inserting t = t2 into (17), ΔiL is obtained for buck-boost operation as.

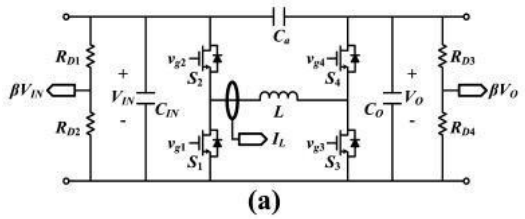
$$\Delta i_L = i_L(t_2) - i_L(t_0) = \frac{V_{IN}}{L} DT_S, \quad (23)$$

where $DT_S = t_2 - t_0$. Because $\langle i_L \rangle = I_{IN} + I_O$ and $i_L(t_0) = \langle i_L \rangle - \Delta i_L/2$, $i_L(t_0)$ is expressed as

$$i_L(t_0) = I_{IN} + I_O - \frac{V_{IN}}{2L} DT_S, \quad (24)$$

and $i_L(t_2) = \langle i_L \rangle + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_{IN} + I_O + \frac{V_{IN}}{2L} DT_S. \quad (25)$$



(a)

The ESR loss of capacitor (PC,ESR) is expressed as CESRC rms RIP where IC,rms is the RMS value of the capacitor current, and RC is the ESR of the capacitor. The voltages and currents of the key power components for calculating these power losses have different values for the different operating modes

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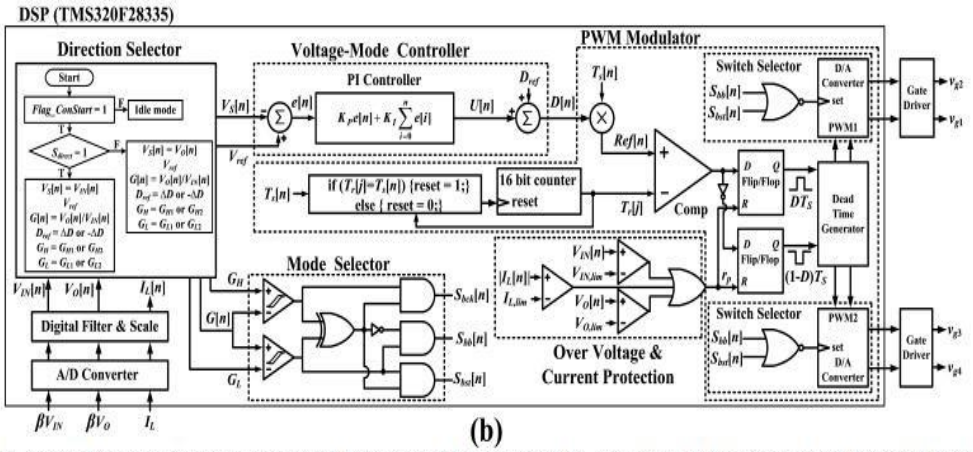

Fig. 11. (a) Circuit structure of the proposed converter with the voltage and current sensing (βV_{IN}, βV_O, and I_L), (b) Block diagram of the digital controller for the proposed converter.

(Table II). The theoretical efficiency of the proposed converter can be calculated by inserting voltage and current values into the equations related to the power loss calculations.

F. Operation of the Controller

The proposed converter is controlled by pulse width modulation (PWM) signals (vg1 ~ vg4), which are generated by the voltage-mode control (Fig. 11(a)). Two voltages (VIN and VO) are sensed to implement the voltage-mode control and protect the over voltage. VO is used as an output voltage for generating the PWM control signal of the main switch in the energy transfer direction from VIN to VO, and VIN is used as an output voltage in the opposite direction. The current of inductor is sensed to protect against over current. Fig. 11(b) represents a block diagram of the digital controller for the proposed converter. When the energy transfer direction is expressed by the demand of the system, the direction selector determines the sensing output voltage (VIN or VO) needed for the voltage mode control. The voltage-mode PI controller then generates the duty ratio D of the main switch by comparing the sensed voltage with the reference voltage. The mode selector informs the PWM modulator of the operating mode of the proposed converter determined by the sensed VIN and VO. Finally, using the information from the mode selector and voltage mode controller, the PWM modulator and the switch selector generates four gate signals (vg1 ~ vg4), which control the proposed converter. The proposed converter has six operating conditions that depend on the energy transfer direction and operating modes (Table I). In each energy transfer direction, one of three operating modes is used (buck, boost,)

buck-boost ↔ boost). Hysteresis control and the switch selector are used to solve this problem. The hysteresis control uses different gains (GL1, GL2, GH1, GH2) for smooth transition between modes, and the switch selector determines the main switch that controls the operation and voltage gain G (= VO / VIN) of the converter in each mode (Fig. 12).

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TABLE II
VOLTAGE AND CURRENT OF THE KEY POWER COMPONENTS FOR CALCULATING FIVE MAIN CAUSES OF POWER DISSIPATION

Five main causes of power dissipation	Operating modes		
	Buck mode	Boost mode	Buck-Boost mode
Switching loss of switch	$V_{S1,turn-off} = V_{S2,turn-off} = V_{IN}$ $I_{S1,turn-off} = -I_O + \frac{V_{IN}-V_O}{2L}DT_S$ $I_{S2,turn-off} = I_O + \frac{V_{IN}-V_O}{2L}DT_S$	$V_{S3,turn-off} = V_{S4,turn-off} = V_O$ $I_{S3,turn-off} = I_{IN} + \frac{V_{IN}}{2L}DT_S$ $I_{S4,turn-off} = -I_{IN} + \frac{V_{IN}}{2L}DT_S$	$V_{S1,turn-off} = V_{S2,turn-off} = V_{IN}$ $V_{S3,turn-off} = V_{S4,turn-off} = V_O$ $I_{S2,turn-off} = I_{S3,turn-off} = I_{IN} + I_O + \frac{V_{IN}}{2L}DT_S$ $I_{S1,turn-off} = I_{S4,turn-off} = -I_{IN} - I_O + \frac{V_{IN}}{2L}DT_S$
Conduction loss of switch	$I_{S1,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S2,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = I_{L,rms}$	$I_{S3,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S1,rms} = I_{L,rms}$	$I_{S1,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S2,rms} = \sqrt{D}I_{L,rms}$ $I_{S3,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = \sqrt{1-D}I_{L,rms}$
Winding loss of inductor	$I_{L,rms} = \sqrt{I_O^2 + \frac{V_{IN}-V_O}{12L}DT_S}$	$I_{L,rms} = \sqrt{I_{IN}^2 + \frac{V_{IN}}{12L}DT_S}$	$I_{L,rms} = \sqrt{(I_{IN}+I_O)^2 + \frac{V_{IN}}{12L}DT_S}$
Core loss of inductor	$\Delta i_L = \frac{V_{IN}-V_O}{L}DT_S$	$\Delta i_L = \frac{V_{IN}}{L}DT_S$	$\Delta i_L = \frac{V_{IN}}{L}DT_S$
ESR loss of capacitor	$I_{Ca,rms} = I_{Co,rms} = \frac{V_{IN}-V_O}{4\sqrt{3}L}DT_S$	$I_{Ca,rms} = I_{Co,rms} \approx \frac{1}{2}\sqrt{1-D}I_{L,rms}$	$I_{Ca,rms} = I_{Co,rms} \approx \frac{1}{2}\sqrt{1-D}I_{L,rms}$

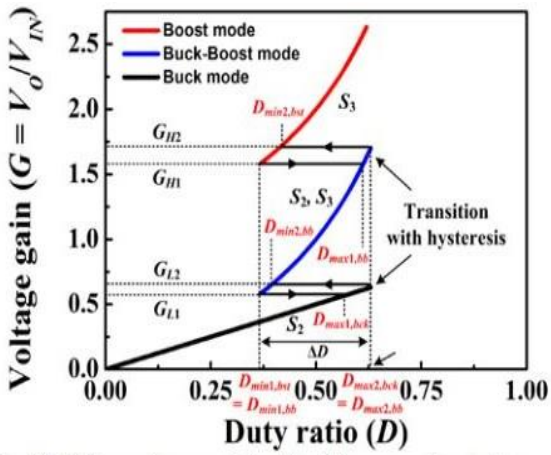

Fig. 12. Voltage gain versus duty ratio of the proposed converter.

Switches SI, S2, S3, and S4 The voltage stress for each switch is VO or VIN, depending on the position of the switch and operating modes. The proposed converter uses four identical power semiconductors as switches.

Therefore, the voltage stress vS,max for a switch is determined as a large value of VIN and VO. The current stresses for the switches change according to the energy transfer directions and operating modes. The maximum current iS,max of a switch is equal to iL(t2), and is expressed in (8), (16), and (25) for buck, boost, and buck-boost operations. The switch component should be chosen to satisfy vS,max < VSwitch and iS,max < ISwitch, where VSwitch and ISwitch are the maximum voltage and current ratings of the switch component.

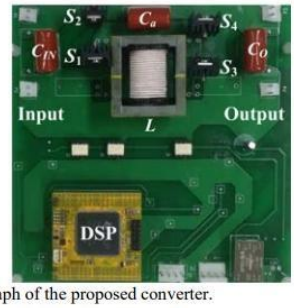

Fig. 13. Photograph of the proposed converter.

TABLE III
VALUES OF COMPONENTS FOR THE EXPERIMENTAL CONVERTERS

Components		Proposed converter	Coventional CBB converter
Core of inductor		EER 4042	EER 4042
Inductor (L)		184 μH	184 μH
Input capacitor (C_{IN})		3.3 μF	3.3 μF
Output capacitor (C_O)		3.3 μF	3.3 μF
Auxiliary capacitor (C_a)		3.3 μF	
Switches	(S_1)	STP28NM60	STP28NM60
	(S_2)	STP28NM60	STP28NM60
	(S_3)	STP28NM60	STP28NM60
	(S_4)	STP28NM60	STP28NM60

V. CONCLUSION :

A new bidirectional buck-boost converter was proposed in this paper. The proposed converter effectively had lower output current ripple than the conventional CBB converter, which was achieved by providing a bypass path for the output current. The reduced output current ripple enabled lower output voltage ripple and higher power-conversion efficiency compared to the conventional converter. The proposed converter had a maximum efficiency of 98% at

VIN = 160 V, VO = 80 ~ 320 V, PO = 16 ~ 160 W, and fS = 45 kHz, and the output voltage ripple was less than 5.14 Vp.p. These results show that the proposed converter is suitable for PV-ESS in a smart grid, which requires a bidirectional buck-boost converter with high efficiency and low ripples in the output voltage and current.

FUTURE SCOPE:

The Fuzzy based bidirectional buck-boost converter enhances the stability of the system and improves the dynamic response of the system operating in a better way and it has also effectively enhanced the damping of bidirectional buck-boost converter simulation results.

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