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Novel Common-Ground Single-Phase Five-Level Transformer less Boost Inverter for Photovoltaic Applications

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Abstract — This paper presents a transformerless five-level boost inverter with a common ground connection for single-phase photovoltaic (PV) systems. It consists of nine switches, two capacitors, and an LC filter at the output. The topology eliminates common mode (CM) leakage current by connecting the negative terminal of the PV directly to the neutral point of the grid, which bypasses the PV array's stray capacitance. As compared to the conventional flying capacitor (FC) multilevel inverter and the cascaded H-bridge (CHB) multilevel inverter, the proposed topology achieves an output voltage that is up to four times higher given an equivalent dc-link voltage. This reduces the dc-link voltage requirement to one fourth of the values used in conventional multilevel inverters (FC, CHB, NPC, ANPC) and one half of the conventional H-bridge topologies. The following manuscript presents the operation principles and theoretical analysis of the proposed topology, which are supported by simulation and experimental results. A 1 kW prototype was constructed; it achieves 96% efficiency operating at an output of 240 VAC, 60 Hz, and 973 W.

Keywords: common mode (CM) current; photovoltaic (PV) system; switched capacitor; transformerless inverter; virtual DC bus.

1. INTRODUCTION

The rate of solar energy deployment has increased rapidly due to concerns for the environment and a reduction in the system-level costs of photovoltaic (PV) systems. In residential applications, the cost of this hardware has decreased 61% between 2010 and 2017 [1]. Yet, there are still many

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opportunities for improvement, especially in the power electronics used in these systems. It is typical to use a transformer in PV applications to provide galvanic isolation between the panel and grid as well as to achieve a high voltage conversion ratio. However, the transformer adds additional weight and cost to the hardware and decreases its efficiency [2]. For these reasons, researchers have examined various transformerless topologies as a means of mitigating these concerns [2]–[5]. Multilevel inverters exhibit some interesting advantages compared to two-level voltage source inverters (VSIs), especially for higher voltage power conversion, where lower switch voltage stress and lower harmonic content exist [6]–[10]. For grid-connected applications, multi-level topologies are more common due to their advantages of improved output current, lower switching losses, and reduced electromagnetic interference (EMI). In multi-level topologies, low-voltage switches can be used instead of high-voltage switches, as in two-level inverters. Low-voltage switches are normally smaller and cheaper and can handle higher switching frequencies. In addition, the conduction losses are reduced due to a lower forward-voltage drop, and the switching loss is reduced due to the smaller dv/dt. Furthermore, two-level topologies need to switch more often than multi-level topologies to achieve the same output quality. Thus, the switching frequency can be reduced in multi-level topologies, thereby reducing the associated switching losses. Furthermore, multi-level topologies offer more than two voltage levels, and this improves the output voltage waveform by better approximating a sine wave. Despite the advantages listed above, the main drawback of multilevel inverters is the requirement of a higher dc-link voltage (two times the peak ac output voltage for most of the NPC, ANPC, and FC family topologies). This requires an additional front-end step-up dc-dc converter or a string of series-connected PV modules to lift the dc-link voltage from 400 V to 800 V for active power control on the grid. While this can be done with an inductive-based boost converter, switch-capacitor circuits also offer boost functionality while being able to maintain a higher power density than converters that employ magnetic elements. [11]-[12]. Recently, the advantages of switched-capacitor topologies have been demonstrated in PV applications [13]–[15]. Considering these aspects, a novel common ground-type five-level single-phase boost inverter is investigated in this paper for PV

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applications. It reduces the dc-link voltage requirements up to ¼ of the value in conventional multilevel topologies and ½ of the value in traditional H-bridge inverters. The common mode leakage current to the grid is eliminated by connecting the negative terminal of the PV directly to the neutral point of the inverter.

2. OPERATING PRINCIPLES OF PROPOSED TOPOLOGY

A. Principle of operation

The proposed topology works on the principle of a 'flying capacitor', which is illustrated in Fig. 1. The capacitor CFC is charged to VDC when the switches are in position 1. When the switches are in position 2, it produces an equal and opposite polarity across the terminal AB. During this state, the capacitor is typically discharged. This concept of a flying capacitor has been utilized in various modern common-ground transformerless inverters [2]. The utilization of only capacitors as the primary energy storage elements is beneficial in terms of the overall cost and weight of a power converter, in contrast to the utilization of both capacitors and inductors.

B. Proposed topology

The proposed topology is a transformerless, five-level boost inverter. As shown in Fig. 2a, it utilizes nine switches.

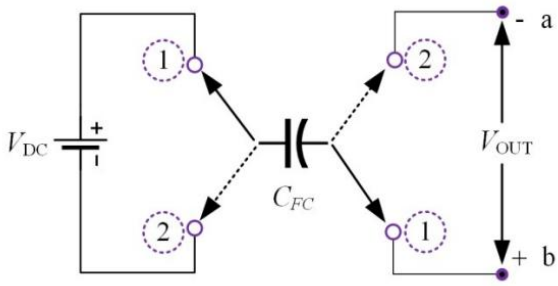
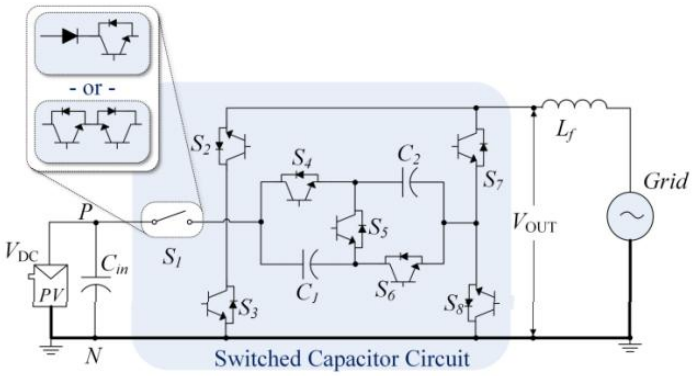


Fig. 1 Principle of operation of virtual DC bus capacitor



and two flying capacitors to realize five discrete output voltages: 2 VDC, VDC, 0, VDC, -VDC, and -2 VDC. To accomplish this, S1 must be bidirectionally blocked. It can be implemented using a back-to-back connection or a device with a reverse blocking diode, as shown in Fig. 2a. During the inverter's operation, the flying capacitors are charged in parallel and discharged in series or parallel, depending on the

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magnitude of the output voltage. Additionally, it is implemented with a common ground connection between the negative terminal of the photovoltaic panel (PV) and the neutral connection of the grid. This eliminates the common mode leakage current since the PV's parasitic capacitance is bypassed. The control strategy for the inverter is shown in Fig. 2b. A traditional multi-carrier approach is used where the switching signals are generated by comparing four carrier waves (vP2, vP1, vN1, and vN2) to a reference waveform (vREF):

$$v_{REF}(\theta) = 2m_a \sin(\theta),$$

where θ = ωc ·t, ωc is the angular frequency, and ma is the modulation index. Thus, the RMS value of output voltage (VOUT) for the proposed topology is:

$$V_{OUT} = \frac{2 \cdot m_a \cdot V_{DC}}{\sqrt{2}}.$$

The operation of the inverter can be broken up into four regions that correspond to a specific range of values for the reference waveform. The relationship is given in Table I and illustrated in Fig. 2b. For each region of operation, the inverter switches between two different states. Most of the switches are

TABLE I. REGION OF OPERATION FOR THE PROPOSE TOPOLOGY

Region	v_{REF}	Low State	High State
1	$1 < v_{REF}(\theta) \leq 2$	A (+ V_{DC})	B (+ $2V_{DC}$)
2	$0 < v_{REF}(\theta) \leq 1$	C (0)	A (+ V_{DC})
3	$-1 < v_{REF}(\theta) \leq 0$	D (- V_{DC})	C (0)
4	$-2 < v_{REF}(\theta) \leq -1$	E (-2 V_{DC})	D (- V_{DC})

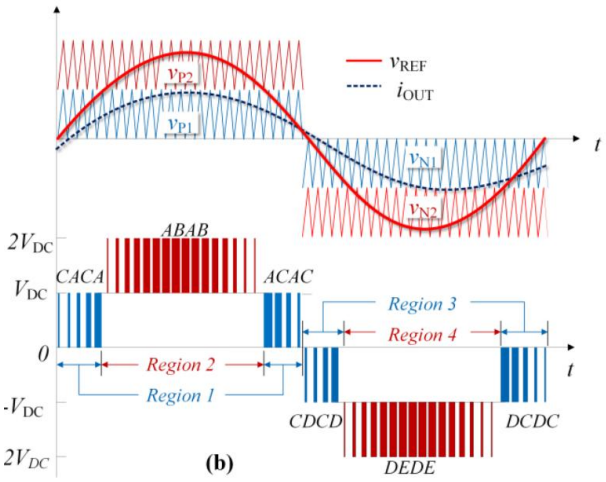

Fig. 2 The proposed 5-level transformerless inverter's (a) circuit diagram and (b) the corresponding PWM modulation scheme.

static, while either two or three are modulated using SPWM to produce the output. During Region 1, S2 and S7 are complimentary, and the remaining switches are static. The inverter switches between 0 and VDC. In Region 2, S4 and S6 switch together and are complements of S5. During Region 3, S3 and S8 are complimentary. In Region 4, S4 and S6 are complements of S5, just like in Region 2. The capacitors are fully charged once per cycle. As explained

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in the next section, charging occurs during State A and State C when the output voltage is +VDC and 0VDC, respectively. However, to realize the +2 VDC output and the negative output states, the capacitors will function as a virtual DC bus [3]. Furthermore, it can be seen that charging does not occur during Region 4. Therefore, the capacitors' voltage will decrease during this time, and the capacitors will need to be sized according to the output power, the fundamental frequency, and the capacitor's ripple voltage requirements.

3. OPERATING MODES OF THE PROPOSED TOPOLOGY

The proposed inverter has five operating states, as shown in Fig. 3. The status of the switches during each state and the corresponding output voltage are given in Table II. Each state will be described in the subsections to follow. A. State A (+1 level): Fig. 3a shows State A. In this state, the output of the inverter before the filter is +VDC. The capacitors C1 and C2 are charged in parallel through the switches S1, S4, S6, and S8. During this state, C1 and C2 also act as additional dc-link capacitors. In Region 1, State A occurs when vREF is greater than vP1. In Region 2, it occurs when vREF is less than vP2. B. State B (+2 level): State B is shown in Fig. 3b; it is only utilized in Region 2. It produces a voltage level of +2 VDC at the filter's input by connecting the pre-charged capacitors (C1 and C2) in series via S5. To prevent a short circuit to the capacitors, S4 and S6 are off. It is active when vREF is greater than vP2.

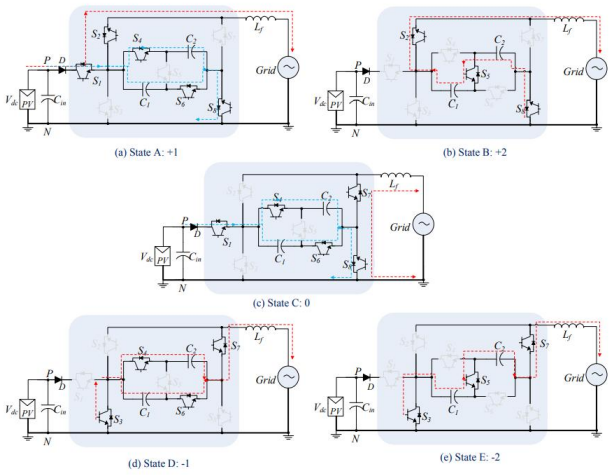

Fig. 3 Five switching states of the proposed 5-level transformerless inverter.

State C (0 level): State C, shown in Fig. 3c, is utilized in Regions 1 and 3. The switches S7 and S8 are closed to form a bidirectional path for current to flow during both the positive and negative cycle zero states. This leads to a zero voltage being applied before the output filter. The switch S2 is off during this state, which allows the capacitors to be charged in parallel through switches S1, S4, S6, and S8. S5 is off in this state to prevent short-circuiting of the capacitors. In Region

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1, State C occurs when vREF is less than vP1, and in Region 3, it is active when vREF is greater than vN1. D. State D (-1 level): Fig. 3d shows State D, in which the capacitors C1 and C2 are connected in parallel to provide a dc-link voltage of -VDC. During this mode, S3, S4, S6, and S7 are on, and S5 and S8 are off. Assuming C1 and C2 are equal, the grid current (IOUT) splits equally between the two capacitors. Switch S1 is off during this state to prevent a short on the DC input. Switch S2 remains off for the complete negative cycle. In Region 3, State D is active when vREF is less than vN1, and in Region 4, it takes place when vREF is greater than vN2. E. State E (-2 level): This switching state (see Fig. 3e) is similar to State B, in which the capacitors are connected in series to boost the voltage level. However, S1, S2, and S8 are off, S3 and S7 are on, and the capacitors are connected with reverse polarity to the output filter. As in State B, by turning off S4 and S6 and turning on S5, the capacitors are connected in series rather than parallel to the output filter, doubling the voltage. During this mode, the current in C1 and C2 is equal to IOUT. The result is -2 VDC applied to the output filter. State E occurs during Region 4 when vREF is less than vN2. F. Voltage Stress on Transistors: The voltage stress on the transistors is not symmetrical. Upon examining the schematics for State B and State E, it can be seen that some of the transistors have to block twice as much VDC. On the other hand, some of the transistors must only block VDC. The ratings for each switch are summarized.

4. SIMULATION RESULTS

The proposed topology was simulated using Matlab Simulink and the PLECS toolbox in order to validate its performance. The waveforms are shown in Fig. 4. It can be seen that the inverter takes 200 V and is able to produce a five-level output voltage that can be filtered to produce sinusoidal voltage and current waveforms. Furthermore, a small drop in the capacitors' voltage appears during Region 4. Finally, the voltage stress for each of the switches is easily discernible. Several points should be considered. First, it can be seen that S1 needs to block bidirectional voltage. Second, the voltage stress for each switch corresponds to the values

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Fig. 5 Modular prototype inverter with two provisional capacitor banks.

Parameter/Description	*Value*
Rated Power, P	1 kW
Input voltage, v_{in}	200 V_{DC}
Output voltage, v_{ac}	240 V_{RMS}
Modulation Index, m_a	0.8485
Switching frequency for SPWM, f_S	20 kHz
Line frequency	60 Hz
Load (Resistive)	~ 57 Ω
LC filter	0.37 mH, 2.4 µF
Flying Capacitors (C_1 & C_2)	(4) 100 µF Film (2) 820 µF Elect.
Power switches	Si MOSFET IPP60R125P6

A prototype was developed to validate the operation principles of the inverter; it is shown in Fig. 5. The relevant parameters are given in Table IV. All nine power switches are implemented using 600 V Si MOSFETs. They are attached on the bottom side of the board to a common heatsink that is cooled with a small fan. The flying capacitors are implemented using a combination of film capacitors and electrolytic capacitors. The prototype was constructed to be modular so that the capacitor banks can be interchanged to evaluate the proposed topology in applications outside of grid-tied PV integration. The control signals were generated by a Texas Instruments Peripheral Explorer Kit that uses a TMS320F28335 digital signal processor (DSP). Testing was performed at the rated power level (see Tables IV and V). A resistive load bank was used in place of a grid-tied connection to simplify the implementation. The experimental results are shown in Fig. 6 for the

inverter.

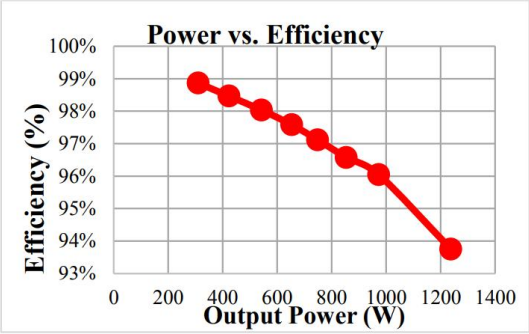

Figure 6: Plot of power vs. efficiency (VDC = 200 V, VLOAD = 240 VRMS).

operating at a load of nearly 1200 W. The figure shows the DC input voltage (VDC), the output voltage before (VOUT) and after the filter (VLOAD), and the load current (ILOAD). It can be seen that the filtered voltage and current are clean sinusoidal waveforms. Additionally, the inverter's output shows five discrete levels with minimal change in the DC link voltage during region four. The results confirm that the inverter is able to operate at rated load and produce clean output waveforms. Efficiency measurements were made from 300 W to 1200 W using a high-precision power analyzer (p\n: Hioki PW3390) and two current clamps. The maximum

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efficiency was 99%; it occurred at 30% of the load. At the rated power level of 1 kW, the efficiency was 96%. Beyond this point, the efficiency begins to drop rapidly as some of the devices operate at the edge of their safe operating area. This was noticeable at 1200 W because the temperature on S1 rose quickly. Table V includes the measurement values obtained using the power analyzer.

5. CONCLUSIONS

The following paper proposes a new topology for single-phase photovoltaic (PV) systems. It is a transformerless, 5-level boost inverter with a common ground connection and two flying capacitors. The operating principles of the inverter are given for each of the five switching states. Next, the derivations were supplied to show how to size the flying capacitors for a given input voltage, output voltage, output power, and capacitor ripple requirements. This was followed by basic simulation results. Finally, the paper concluded with experimental results at rated voltage and power. It was demonstrated that the inverter can operate with very high efficiency (~99%) at light loads while still achieving an efficiency of 96% at 1 kW.

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