DESIGN OF SHIFT REGISTERS USING MAJORITY LOGIC BASED QCA TECHNOLOGY

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ABSTRACT: A quantum dot cellular automaton (QCA) is an emerging technology developed at Nano metric scale, which has lower area such as programmable logic blocks (PLB) requirement and low Power Consumption, quantum cells. Most of the integrated circuits are developed using CMOS technology with the higher physical area dimensions, QCA approach proves to one of the potential arrangements in beating this physical layout. In this article, various sequential circuits are designed such as D-FLIP FLOP (FF), Serial-in-serial-out (SISO), Serial-in-parallel-out (SIPO), Parallel-in-parallel-out (PIPO), and parallel -in-serial-out (PISO) shift registers. The implementation and simulation results developed using Xilinx ISE simulation tool and results shows that the proposed designs provide the enhanced results compared to the conventional approaches with respect to the delay (speed), power utilization and hardware utilization.

1. INTRODUCTION

Advancements in VLSI have been done on three variables: area and Delay, power. Area improvement implies decreasing the space of rationale which possess on the pass on. This is done in both front-end and back-finish of structure. In front-end structure, legitimate portrayal of rearranged Boolean articulation and expelling unused states will prompt limit the door/transistor utilization. Segment, Floor arranging, Placement, and directing are act in back-finish of the plan which is finished by CAD tool[1].The CAD instrument have a particular calculation for each procedure to create a zone proficient structure like Power advancement. Force streamlining is to lessen the force dissemination of the plan which endures by working voltage, working recurrence, and exchanging movement. The initial two components are simply indicated in plan imperatives however exchanging action is a parameter which fluctuates powerfully, in light of the way which designs the rationale and information vectors. Delay improvement alludes to meeting the client imperatives in effective way with no infringement in any case, improving execution of the structure. The fig.1 given below represents a QCA cell. The four dots of quantum cell represents holes and electrons. White colored dots represent holes and black colored dots represent electrons. Thus, there are four dots in QCA quantum cell out of which two are filled with electrons and two are filled with holes and now if we apply charge, the two electrons are free to occupy any hole and thus

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we can have two different combinations of holes and electrons in as illustrated in fig.1. These two different combinations of holes and electrons are used to represent the two stable states binary 0 and binary 1 in QCA technology.
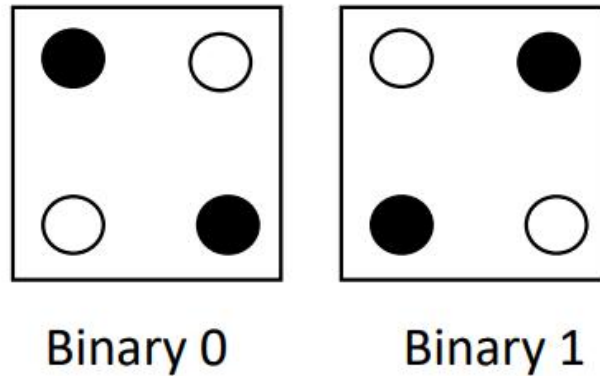

Fig.1: Structure of QCA

The QCA are an appealing rising innovation reasonable for the improvement of ultra-thick low-control elite advanced circuits. Hence, over the most recent couple of years, the plan of productive rationale circuits in QCA has gotten a lot of consideration. Exceptional endeavors are coordinated to number-crunching circuits, with the primary intrigue concentrated on the twofold expansion that is the essential activity of any advanced framework. Obviously, the models regularly utilized in customary CMOS plans are viewed as a first reference for the new structure condition. The CFA was an advanced RCA that moderated effects of impending cables. Parallel prefix structures have been dissected and updated in QCA including Bent Kung adder, kogge-stone adder and Han Carlson adder. For the CLA and RCA, increasingly effective structures have been proposed. In this short, an inventive procedure is introduced to execute fast low-zone adders in QCA. Theoretical definitions displayed for CLA and parallel-prefix adders are here mishandled for the affirmation of a novel 2-piece extension cut. The last empowers the bring to be multiplied through two following piece positions with the deferral of just a single larger part MG. Similarly, the sharp top level building prompts traditionalist configurations, as needs be avoiding unnecessary clock stages as a result of long interconnections. A adder arranged as proposed continues running in the RCA style, yet it shows a computational concede lower than all condition of the-workmanship contenders and accomplishes the most decreased ADP.

Rest of the paper organized as follows section 2 gives the detailed analysis of conventional methods and its problems. Section 3 gives the detailed analysis of proposed D- FF, shift registers and universal counters with respect to the various block level operations using majority logic formulations. Section 4 gives the detailed analysis of Xilinx ise based software simulation of the proposed method with area, power and delay analysis with simulation waveforms and comparative analysis with various literatures. Section 5 concludes the paper with possible future studies.

2. LITERATURE SURVEY

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FLIP-FLOPS (FFs) [1] are fundamental stockpiling components utilized broadly in computerized framework plans, which receive serious pipelining procedures and utilize a few FF-rich modules, for example, register records, move registers, and FIFO. The force utilization of the FFs utilized in a regular computerized framework plan, alongside that of clock conveyance systems, comprises as high as 20%–45% of the absolute framework power. FF plans are in this manner basic to the force utilization execution of the framework structure and may likewise significantly affect the chip territory. FF structures experience ceaseless improvement with the advances in new procedure innovation. Explicit application requests, for example, rapid, low force, and low voltage likewise call for new FF structures. Albeit various FF[2-3] plans have been created, late structure accentuations have exchanged steadily from ultrahigh-speed flipping to amazingly low-control tasks. Notwithstanding the exchanging power, the spillage power utilization ought to be decreased. The structure is likewise expected to work appropriately for voltage settings underneath the ostensible voltage. Right now, low-power FF configuration meeting these prerequisites is explored. In DET FF[4-5], a regular positive-edge-activated flip-flop (FF) faculties and reacts to the control info or contributions at the time the clock input is changing from 0 to 1. It doesn't react at all to alters in the contrary course. Negative-edge-set off FF's act in an integral way. Therefore, these FF's[6-7] can react all things considered once per clock beat cycle. It is suggested that twofold edgeactivated (DET) FF's, reacting to the two edges of the clock heartbeat would have points of interest as for speed and vitality scattering. In Double edge activating strategy, this technique can be utilized to spare the half of the force on the clock appropriation organize. It utilizes the half recurrence on the tickers conveyance organize by cutting the recurrence of the clock by one half will parts the force utilization on the clock dispersion arrange. Multiple literatures have been studied about flip-flops using QCA[8] because they are estimated to be utilized for developing and analysis in real time sequential logics, for example processers and controllers. In literature [9], QCA based R-S flip-flop was developed. In literature [10] D flip-flop and T flip flop was developed. But this methods does not require any gated clock signals, it only 2-input pins namely reset and set, thus it acts more as latch instead of flip flops.
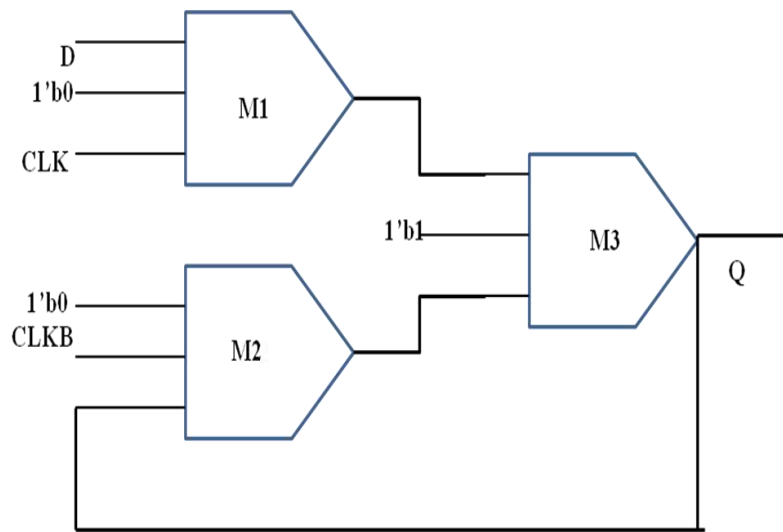
3. PROPOSED METHOD

Fig 2.D-FF using Majority gates

The above figure 2 represents QCA based DFFs using majority formulations. The M1, M2 are functions as AND operation, M3 functions as OR gate. From the M1 data input D is transferred as output using posedge of clock, from the M2 gate previous state of Q is transferred as M2 output using negedge of clock, across M3 both clock triggered outputs are added and gives final output of present state Q.
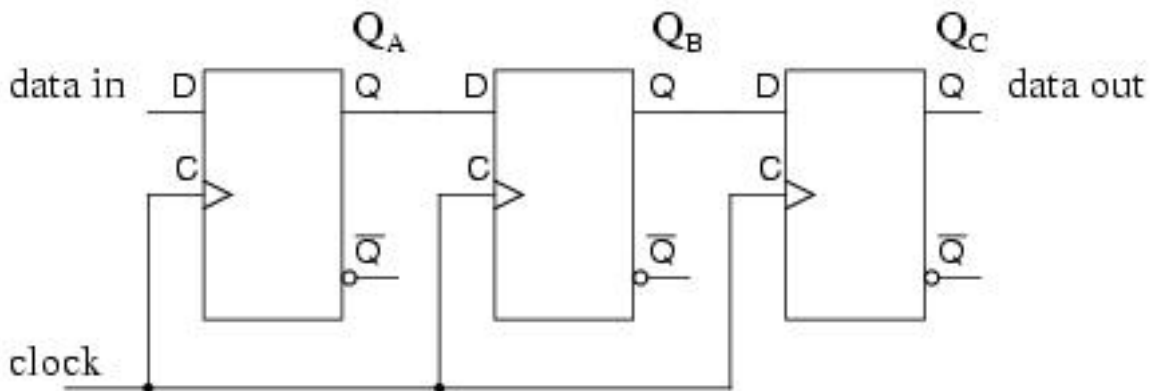

Fig 3. 4-bit SISO shift register using QCA

The 4-bit synchronous shift register consisting of the 4-QCA D-FFs and clock-input of all flip-flops are allied to single base clock. All FFs are edge controlled and the outputs alter synchronously with respect to clock, so it will also act as serial input and parallel output. So, the present output (Q) of first 1st D-FF is straightforwardly connected as data input to 2nd D-FF. similarly, for N-bit shifting operation connections will be same. The shift register output observed across all flip flop's present states Q at once, and arranged in LSB to MSB format.
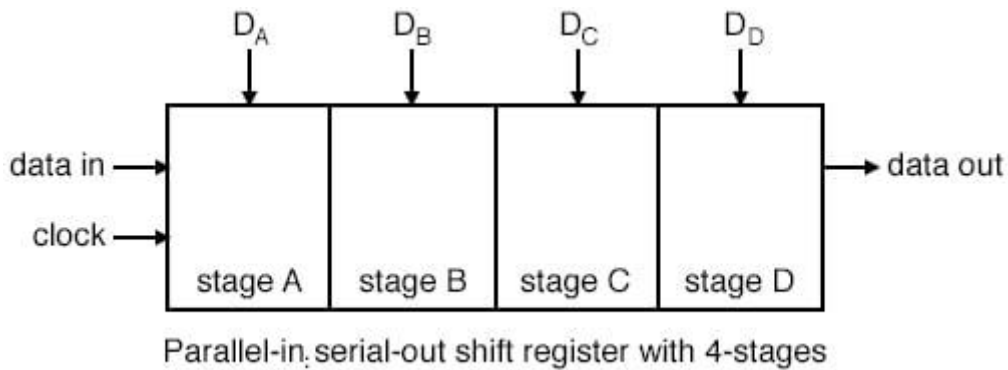
Figure 4. 4-Bit PISO shift register.

Parallel-in/ serial-out shift registers do everything that the previous serial-in/ serial-out shift registers do plus input data to all stages simultaneously as shown in Figure 4. The parallel-in/ serial-out shift register stores data, shifts it on a clock-by-clock basis, and delays it by the number of stages times the clock period. In addition, parallel-in/ serial-out really means that we can load data in parallel into all stages before any shifting ever begins. This is a way to convert data from a *parallel* format to a *serial* format. By parallel format we mean that the data bits are present simultaneously on individual wires, one for each data bit as shown in Figure 4. By serial format we mean that the data bits are presented sequentially in time on a single wire or circuit as in the case of the "data out" on the block diagram in Figure 4. we show the parallel load path when SHIFT/LD' is logic low. The upper NAND gates serving D_A D_B D_C are enabled, passing data to the D inputs of type **D** Flip-Flops Q_A Q_B D_C respectively. At the next positive going clock edge, the data will be clocked from D to Q of the three FFs. Three bits of data will load into Q_A Q_B D_C at the same time. The type of parallel load just described, where the data loads on a clock pulse is known as *synchronous load* because the loading of data is synchronized to the clock. This needs to be differentiated from *asynchronous load* where loading is controlled by the preset and clear pins of the Flip-Flops which does not require the clock. Only one of these load methods is used within an individual device, the synchronous load being more common in newer devices.
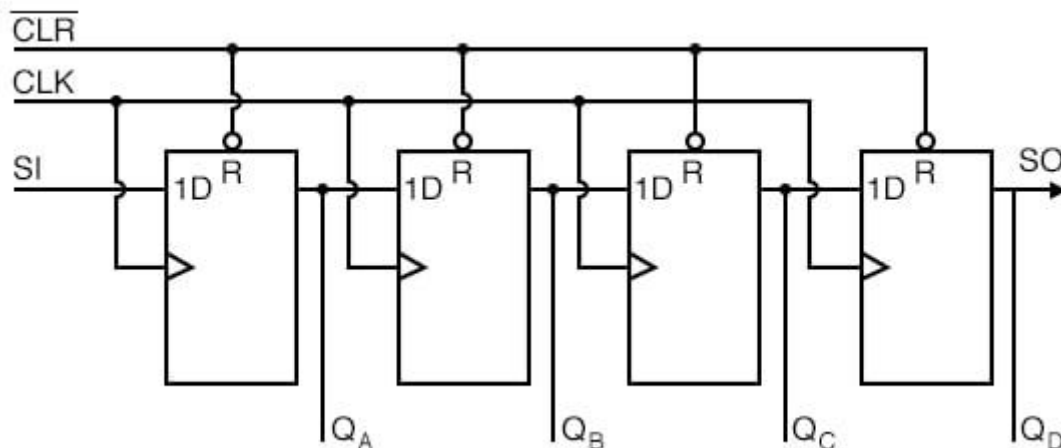
Figure 5. 4-bit SIPO shift register.

A serial-in, parallel-out shift register is similar to the serial-in, serial-out shift registers as shown in Figure 5, that it shifts data into internal storage elements and shifts data out at the serial-out, data-out, pin. It is different in that it makes all the internal stages available as outputs. Therefore, a serial-in, parallel-out shift register converts data from serial format to parallel format. The shift register has been cleared prior to any data by **CLR'**, an active low signal, which clears all type D Flip-Flops within the shift register. Note the serial data **1011** pattern presented at the **SI** input. This data is synchronized with the clock **CLK**. This would be the case if it is being shifted in from something like another shift register, for example, a parallel-in, serial-out shift register. On the first clock at **t1**, the data **1** at **SI** is shifted from **D** to **Q** of the first shift register stage. After **t2** this first data bit is at Q_B. After **t3** it is at Q_C. After **t4** it is at Q_D. Four clock pulses have shifted the first data bit all the way to the last stage Q_D. The second data bit a **0** is at Q_C after the 4th clock. The third data bit a **1** is at Q_B. The fourth data bit another **1** is at Q_A. Thus, the serial data input pattern **1011** is contained in (Q_D Q_C Q_B Q_A). It is now available on the four outputs. It will available on the four outputs from just after clock **t4** to just before **t5**.
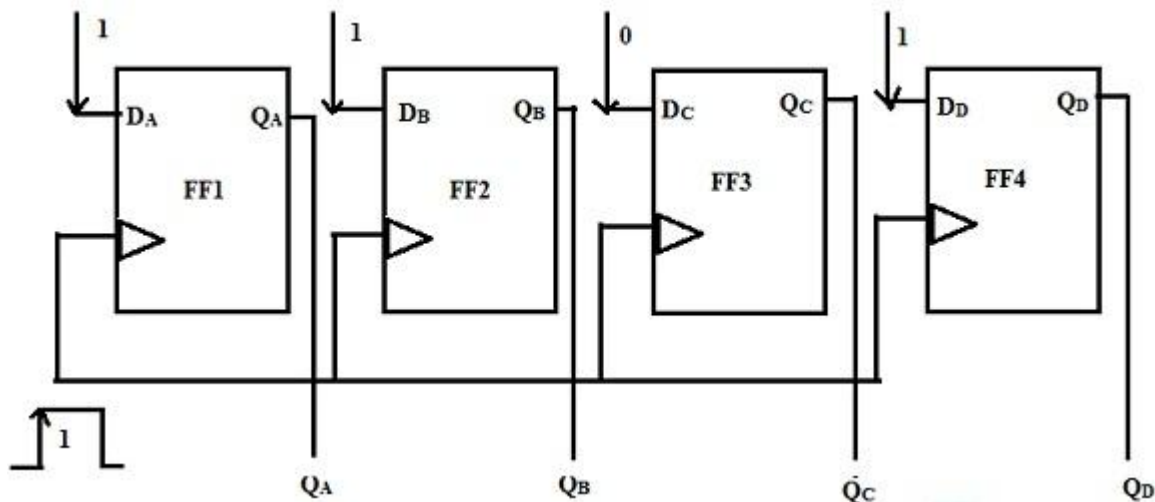

Figure 6. 4-bit PIPO shift register.

The shift registers which uses parallel input and generates parallel output is known as the parallel input parallel output shift register as shown in Figure 6. This shift register includes three connections only the PI (parallel i/p), PO (parallel o/p) & the CLK signal. This kind of shift register also works like a time delay device or temporary storage device like a SISO shift register with the time delay being changed through the CLK signals frequency. In this type of register, the data is available in parallel format with respect to the parallel i/p pins like PA to PD & after that, it is transferred directly together to their respective o/p pins from QA to QDby the similar CLK signal. After that single CLK signal will load & unload the shift register. The circuit diagram of the PIPO shift register is shown below. The input allowed by this type of shift register is parallel & gives a parallel output. This logic circuit is designed

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with 4 D-FFs which is shown in the diagram. In this circuit, both the CLR and CLK signals are connected to 4 D FFs.

4. SIMULATION RESULTS:

All the proposed designs have been programmed and designed using Xilinx ISE software this software tool provides the two categories of outputs named as simulation and synthesis. The simulation results give the detailed analysis of proposed design with respect to inputs, output byte level combinations. Through simulation analysis of accuracy of the addition, multiplication process estimated easily by applying the different combination inputs and by monitoring various outputs. Through the synthesis results the utilization of area with respect to the programmable logic blocks (PLBs), look up tables (LUT) will be achieved. And also time summary with respect to various path delays will be obtained and power summary generated using the static and dynamic power consumed.
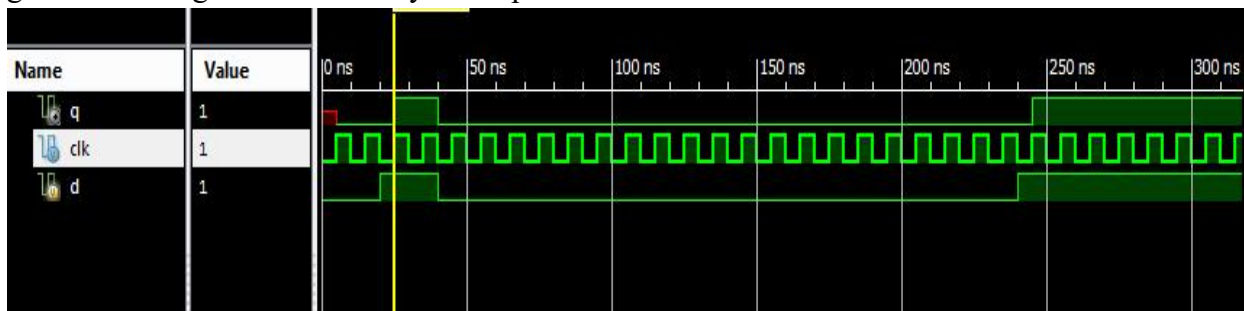

Figure 7. simulation output of D-FF

The above figures represent the simulation of waveforms by using the Xilinx ISE software for flip flops.

Table 1: Comparison of Flip-Flops

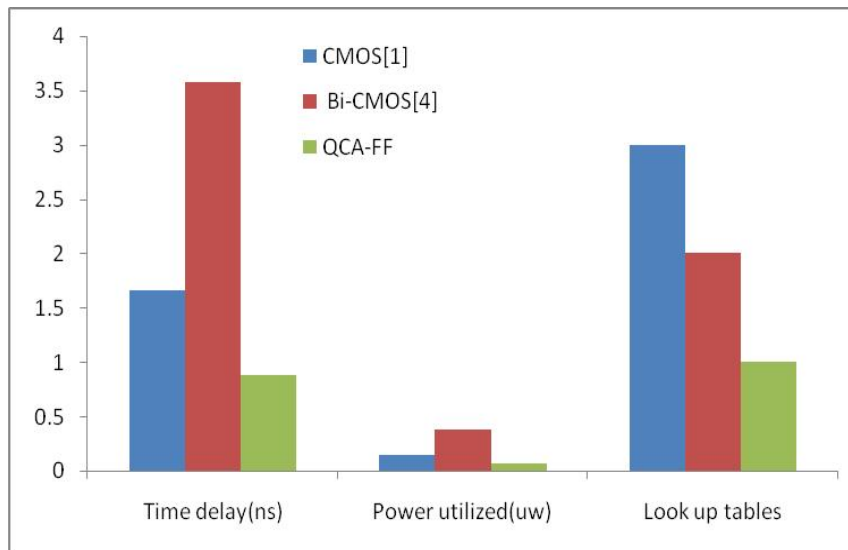| Parameter	CMOS [1]	Bi-CMOS [4]	PROPOSED QCA-FF
Time delay(ns)	1.664	3.573	0.882
Power utilized(uw)	0.143	0.384	0.065
Look up tables	3	2	1

Figure 8: Comparison of Flip-Flops

Table 2: Comparison of Shift registers

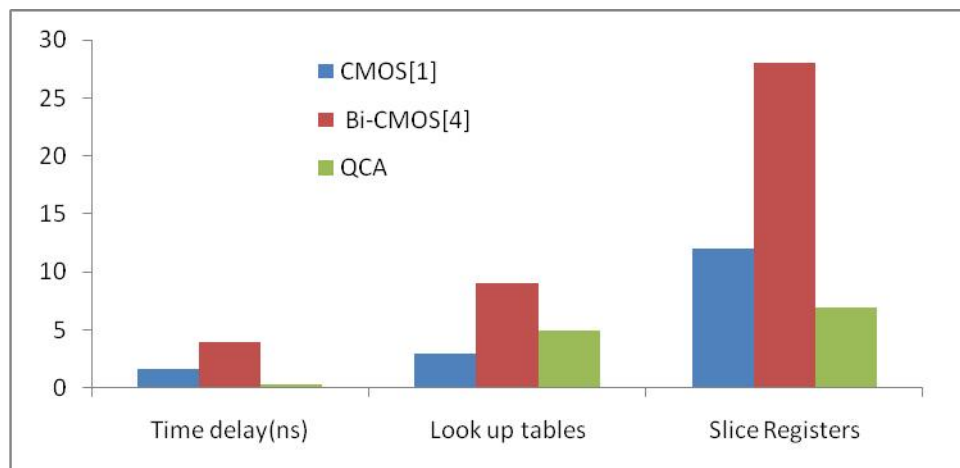| Parameter	CMOS [1]	Bi-CMOS [4]	PROPOSED QCA-Shift registers
Time delay(ns)	1.664	3.929	0.356
Power utilized(uw)	0.143	0.065	0.011
Look up tables	3	9	5
Slice Registers	12	28	07

Figure 9: Comparison of Shift registers

From table1, table 2, table 3 and Figure 9, figure 10, figure 11; it is observed that the proposed flip flops, and SISO, SIPO, PISO, PIPO-shift registers developed using QCA showing enhanced area, power and delay properties compared to the conventional approaches CMOS [1] and Bi-CMOS [4].

5. CONCLUSION

In this work, a new method of implementing flip-flops, counters and shift registers with smaller amount hardware, area intricacy in nanotechnology. Any storage memory can develop utilizing with these proposed flip-flops, and various shift registers. The mahority gate designs has been created and simulated using various combinations, finally outputs are generated using Xilinx ISE simulation software. The permanence of the proposed method has been showed better results with respect to area, power and delay compared to conventional approaches.

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