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AN INVESTIGATION INTO THE RF PERFORMANCE OF SURROUNDING GATE MOSFETS WITH GATE OVERLAP AND UNDERLAP

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ABSTRACT: This study investigates the RF performance of surrounding gate (SRG) MOSFETs using a simulation exercise. It has also been carefully examined how non-ideality in the fabrication process leads to a nonsymmetrical gate structure. A 2D device simulator is used to investigate important RF figures of merit, such as the maximum operating frequency (fMAX) and the unity-gain cut-off frequency (fT). There have also been reports on the trends in the fluctuation of numerous design parameters, such as radius, oxide thickness, gate length, and doping, as they downscale.

Keywords: surrounding gate MOSET, RF performance, unity-gain cut-off frequency, maximum operating frequency, gate overlap/underlap

1.INTRODUCTION

The physical size of metal oxide semiconductor field-effect transistors (MOSFETs) has steadily decreased during the last four decades. The performance of scaled devices is primarily controlled by a set of physical features known as short channel effects (SCEs), which occur as the size of MOSFET devices are gradually reduced.

Research is now being performed to investigate the deployment of innovative technologies capable of exceeding the restrictions anticipated by classic planar device building and maintaining the high pace of MOSFET reduction. The surrounding gate nanowire MOSFET is being investigated as a potential alternative to typical silicon planar MOSFET configurations. The surrounding gate nanowire transistor outperforms single-gate devices, making it a good choice for improving complementary metal oxide semiconductor (CMOS) technology.

Surrounding gate metal oxide semiconductor (SRG MOS) devices have recently received a lot of attention due to their exact geometry and the electrostatics of the gate-all-around configuration. These devices have shown the most efficacy in reducing short-channel effects, making them the most promising for further reducing the size of CMOS technology.

Scaling challenges in digital logic applications include the ability to withstand single-event upsets, regulate the flow of leakage currents, increase drain saturation current while lowering power supply voltage, and maintain control over device parameters (such as threshold voltage) within and between chips. Further scaling issues for analog/mixed-signal/RF applications include the necessity for precise transistor matching, increased intrinsic gain, low noise performance, higher unity-gain cut-off frequency, and superior linearity. The transistor's high-frequency capabilities have now reached gigahertz levels, making it appropriate for many radio-frequency (RF) circuit applications. This accomplishment is owing to advancements in scaling down SRG MOS-FET to the deca-nanoscale domain. As a result, in order to create a low noise RF integrated-circuit (IC) design using multiple-gate MOSFET technology, the RF performance must be precisely simulated at each stage of the downsizing process. Extensive study has been conducted on the band structure and transport properties, as well as the effect of process

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variation and design optimization of SRG MOS devices for logic and digital applications. However, there has been very little published research on the RF performance of the SRG MOS chip.

Furthermore, advancements in CMOS technology have made it desirable for system-on-chip (SoC) applications. In these applications, MOS transistors replace the previously dominating bipolar technology in RF circuits. This substitution does not affect RF performance characteristics like maximum operating frequency or unity-gain cut-off frequency. The goal is to lower expenses while improving the performance of RF devices.

As a result, it is critical for innovative device architectures, such as surrounding gate MOSFETs, to meet RF standards, as they are essential components of any System-on-Chip design. To produce a low-cost RF mixed signal CMOS SoC and eliminate the need for additional manufacturing methods, the RF-CMOS device topology should be the same as logic CMOS. Each iteration of scaled CMOS technology has focused on discovering whether low-cost RF mixed CMOS devices can fulfill the demands of high-performance RF applications, such as cellular phones, as a result of changes in logic optimization and RF CMOS device topologies. There is a critical need to examine trends in RF performance attributes as they scale down for the design of low noise RF integrated circuits. This is critical in the field of deca-nanometers and is difficult due to the intricacies involved in developing technologies. Parasitic elements must be accurately removed in order to simulate RF circuits and precisely model intrinsic devices. In addition, the gate resistance must be extracted. While correct modeling of MOSFETs is critical for circuit design, there has been little research on the RF characteristics when scaling down or the physical consequences that can be significantly influenced by device parasitism.

The maximum operational frequency (fMAX) and the unity-gain cut-off frequency (fT) are regarded as the two most essential figures of merit (FOMs) in RF. An SRG MOS device's transconductance is boosted by its superior mobility, resulting in higher operating frequency and current amplification. As a result, SRG MOS nano-scale devices have great promise for use in RF and microwave applications. It is critical to test the compatibility of sub-100 nm SRG MOSFETs for RF applications.

Although the SRG MOSFET has several advantages, its main disadvantage is that it is susceptible to manufacturing process fluctuations, which can have a negative impact on the circuit's overall performance. Among these parameters, gate-source/drain overlap is the most important determinant of SRG device performance variances. The gate-source/drain overlap in SRG MOSFETs has a substantial impact on several device properties. The study looks at how process parameter variations affect gate-source/drain overlap characteristics and the sensitivity of SRG RF performance. This analysis looks at not just traditional device design characteristics like gate length and nanowire radius, but also the feasibility of using gate-source/drain overlap as a design parameter. This study examines the RF performance of surrounding gate (SRG) MOSFETs through simulation analysis. This is the first study to look at the impact of nonsymmetrical gate structures caused by fabrication imperfections.

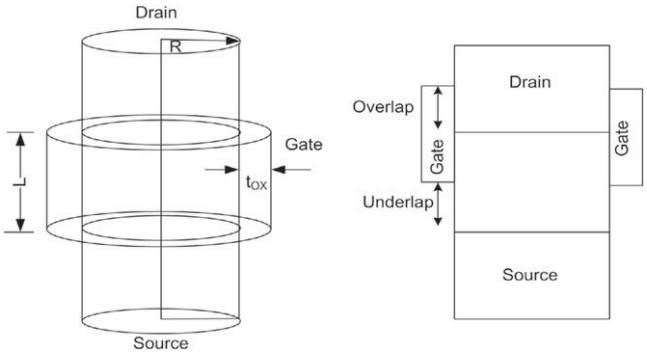

Figure 1. Schematic diagram of SRG MOSFET showing gateunderlap and overlap.

A two-dimensional device simulator is used to investigate the unity-gain cut-off frequency (fT) and maximum operating frequency. The trends in

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the change of various design parameters, such as radius, oxide thickness, gate length, and doping, during the downscaling process are also documented.

2.DEVICE STRUCTURE AND SIMULATION

Figure 1 shows the schematic diagram for the simulated SRG MOSFET. The ATLAS simulator is used to create and model N-channel device topologies in 2D. The device parameters utilized in the simulation were taken from the ITRS roadmap. To account for minority carrier recombination, the simulation uses the CVT model in combination with the SRH and Auger recombination models. In addition, we use the FLDMOB model to account for high field velocity saturation, which is affected by the parallel electric field in the direction of current flow. Furthermore, we use the CONMOB model to describe poor field mobility, which is related to doping density. Gummel's approach, together with Newton's method, is used for carrier transport to solve the equations in the standard drift-diffusion model. To determine the various RF-FOM characteristics at a frequency of 1 GHz, a simulation of an ac small signal device is run over a large frequency range. Each simulation takes into account the oxide thickness (tOX = 2 nm) and the drain-to-source voltage (VDS = 1 volt).

Variable device parameters and their impact on tiny signal RF figures of merit (FOMs) are investigated using RF TCAD simulations. These parameters include the maximum operational frequency (fMAX), which shows RF power performance, and the unity-gain cut-off frequency (fT), which describes a device's overall RF behavior. The maximum operating frequency (fMAX) and the estimated value of the unity-gain cut-off frequency (Ft) are based on

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}\sqrt{1+2C_{gd}/C_{gs}}} \approx \frac{1}{2\pi}\frac{g_m}{(C_{gd}+C_{gs})} \approx \frac{1}{2\pi}\frac{g_m}{C_{gg}}, \quad (1)$$

$$f_{MAX} = \frac{1}{2\pi}\frac{g_m}{2C_{gs}\sqrt{(R_s+R_i+R_g)(g_{ds}+g_m C_{gd}/C_{gs})}}, \quad (2)$$

Given the dispersed nature of the MOSFET, we define Cgs, Cgd, and Cgg as the capacitances between the gate and source, gate and drain, and total gate capacitance, respectively. These capacitances exhibit fringing and overlap effects. Furthermore, gm and gds denote the transconductance and output conductance, respectively, while Rg, Rs, and Ri denote the resistance of the gate, source, and channel (in series with Cgs). Formulae can be used to determine the relationship between fMAX and numerous parameters, including source/drain and gate parasitic resistances, the ratio of miller capacitance to gate capacitance (Cgd/Cgs), and the relationship between fT and the ratio of gm to total gate capacitances. As a result, geometric considerations clearly play an important part in defining the figures of merit (fT and fMAX). To meet the requisite RF standards, increasing fT and fMAX values necessitates reducing parasitic capacitance.

The RF figures of merit (FOMs) are heavily influenced by three major parasitic elements: source/drain (S/D) series resistances, gate parasitic capacitances, and gate resistance. The primary parasitic capacitances in an SRG MOSFET are the overlap capacitance (Cov) and the fringing capacitance (Cfr). Parasitic resistance in silicon-nanowire-tube (SNWT) technology is primarily composed of contact resistance and gate resistance. To accurately estimate the device's performance at high frequencies, the intrinsic gate-engineered MOSFET simulation model must include the gate resistance. This is especially critical when building radio-frequency CMOS circuits operating in the gigahertz range. Several firewalls may be used to reduce resistance at the gate. Alternatively, a silicide technique can lower gate resistance by a factor of ten, and a metal stack procedure can reduce it even further. For our experiment, we employ the usual gate thickness because decreasing the thickness of the gate electrode metals reduces the outer-fringing capacitance Cof while significantly increasing gate resistance. This will have a substantial impact

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on the power consumption and performance of the circuit. Because of its promise as a metal gate technology in the future, we chose to use a 20 nm thick gate electrode made of molybdenum in our simulation study. The metal used in the device has a resistance of 5.2 × 10−6 Ω cm. The effective gate resistance Rg has two components:

1. The effect of the dispersed gate electrode on resistance.
2. Distributed channel resistance Ri is affected by the non-quasi-static (NQS) effect. To calculate the resistance of the scattered gate electrode, we use cylindrical coordinates centered on the cylinder's axis and use a thin cylindrical element with a depth of dR. The resistance of a cylindrical element is defined as

$$dR = \frac{\rho dr}{A}, \quad (3)$$

where A=2 πRL (surface area of the cylindrical element). Integrating equation (3) with r = ra to rb, we obtain

$$R_g = \frac{\rho}{2\pi L} \ln \frac{r_b}{r_a}, \quad (4)$$

where rb − ra is thickness of molybdenum metal gate electrode.

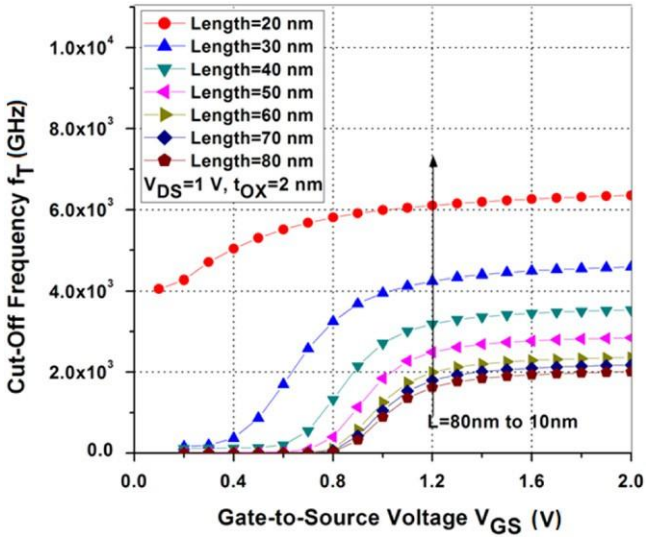

Figure 2. Unity-gain cut-off frequency (f_T) as a function of gate-to-source voltage V_{gs} for different gate length.

Electrical impedance at the junction of the metal and semiconductor. To calculate the contact resistance (Rc) of an SRG MOSFET circuit, use the formula Rc = ρc/A. This assumes that the complete circuit with a radius of R is in direct contact with metal. A denotes the active area of the contact, while ρc represents the specific contact resistance (also known as contact resistivity). This study calculates source/drain contact resistance using the ideal value of 5 Ω μm2. Transistors are typically designed with multiple fingers to generate enough current for multi-gate systems such as SNWTs. Additionally, sources and drains are linked together to share contacts. As a result, the contact resistance has a lower impact on each individual nanowire. Intrinsic resistance (Ri) is proposed to accurately consider the consequences of non-quantum systems (NQS) and deal with them efficiently. This approach adds an additional resistance, Ri, to the current physical gate resistance. The physical gate resistance is now measured at a low frequency or with direct current. Within the strong inversion domain, the value of Ri can be estimated using a simple equation supplied by a Rg model that takes NQS into account.

$$R_i \cong \beta / g_m, \quad (5)$$

where g_m is the transconductance of the device and β is a fitting parameter with a typical value around 0.2.

3.RESULTS AND DISCUSSIONS

Variation of length

Figures 2 and 3 show the relationship between the maximum operating frequency (fMAX) and the unity-gain cut-off frequency (fT) with respect to the gate-to-source voltage Vgs for various channel lengths L. The observed trends indicate that the values of fT and fMAX rise as channel length decreases. Equation (1) shows that when g is not divisible by 1/L m and (Cgs + Cgd) is not divisible by L, the unity-gain cut-off frequency fT has a dependency of 1/L2. Furthermore, fMAX exhibits a 1/L2 dependency as channel length grows. Conversely, as the channel length decreases, the parameters gds and Cgd increase

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and become more prominent, resulting in a slower rate of fMAX expansion.

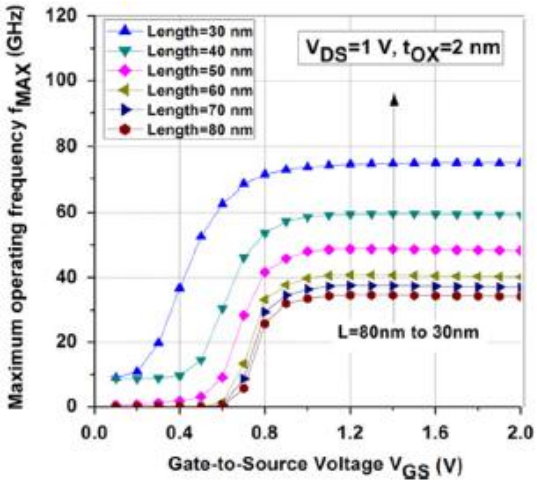

Figure 3. Maximum operating frequency fMAX as a function of gateto-source voltage Vgs for different gate length.

Figures 2 and 3 show that after VGS reaches a certain value known as the threshold voltage, both the unity-gain cutoff frequency fT and the maximum operating frequency fMAX first increase. Following the rise, they reach a greater Vgs saturation point. The fT and fMAX initially grow as the gate bias increases, owing to the combined influence of the faster rise in total gate-to-drain/source parasitic capacitances and the gm restriction imposed by the gate field's loss in mobility. However, after a certain point, both fT and fMAX begin to fall as gate bias grows. The difference between the minimum capacitance at the gate-drain/source and the greatest value of transconductance (gm) correlates to the peak frequency (fT). Because of the consideration, fMAX has a lower value than fT.

The fMAX expression requires the presence of several parasitic elements. The increasing presence of parasitic components considerably reduces the pace at which fMAX increases as channel length decreases.

Variation of radius R

Figure 4 shows how the unity-gain cut-off frequency fT changes as the radius R is reduced. Decreasing R causes an increase in fT. It primarily concerns the idea that, as the channel body widens and the gate electrostatic control on the channel regions weakens, lower gmn can be achieved for a given gate length. As the radius R decreases, the overlap and fringing capacitances grow and become more noticeable. As a result, as the radius R is lowered, the Cgd to Cgs ratio decreases linearly. A larger Cgd/Cgs ratio indicates lower channel charge and more parasitic feedback capacitance. Recently, the underlap channel architecture has been used to improve the Cgd/Cgs ratio due to its ability to reduce parasitic capacitance and provide more gate controllability. When the resistance (R) decreases, the maximum frequency (fMAX) increases due to improved gate control, lower drain-source conductance (gds) caused by thinner nanowires that better mitigate the drain terminal's influence, and an increased ratio of gate-drain capacitance (Cgd) to gate-source capacitance (Cgs).

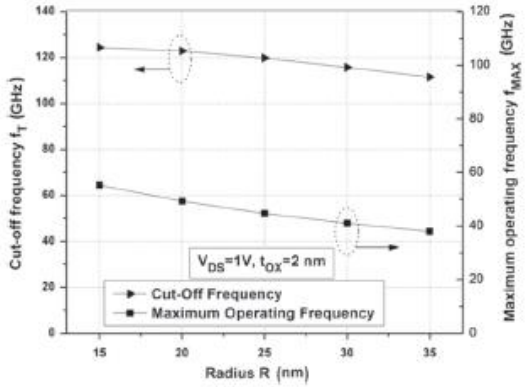

Figure 4. Unity-gain cut-off frequency (fT) and maximum operating frequency (fMAX) as a function of gate-to-source voltage (Vgs) for different values of radius R.

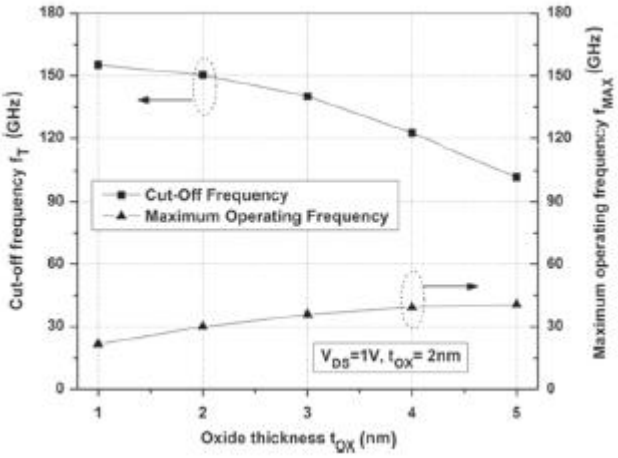

Figure 5. Unity-gain cut-off frequency (fT) and maximum operating frequency (fMAX) as a

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function of various oxide thickness tOX.

Variation of oxide thickness

As the body thickness reduces, the effective gate capacitance increases as the barrier height drops. When electron mobility decreases, both drain current (Id) and transconductance (gm) drop. The variations in fringing capacitance in this situation are mostly due to changes in inner fringing capacitance Cif, whereas outer fringing capacitance Cof remains constant independent of thin body thickness.

As a result, as the body thickness lowers, the overall effective gate capacitance (Cg eff) increases. The usage of intrinsic silicon as a channel helps to reduce mobility loss and improve Ion. According to Equation (2), the only way to obtain good short-channel and RF performance is to thin out the oxide layer (tox). Figure 5 clearly shows the dramatic improvement in device performance that resulted from the reduction of tox. Figure 2 shows that lowering the thickness of the gate oxide significantly increases RF performance in both substantially doped and non-doped channels. As the concentration of tox increases, the effects on threshold voltages diminish, resulting in lower values.

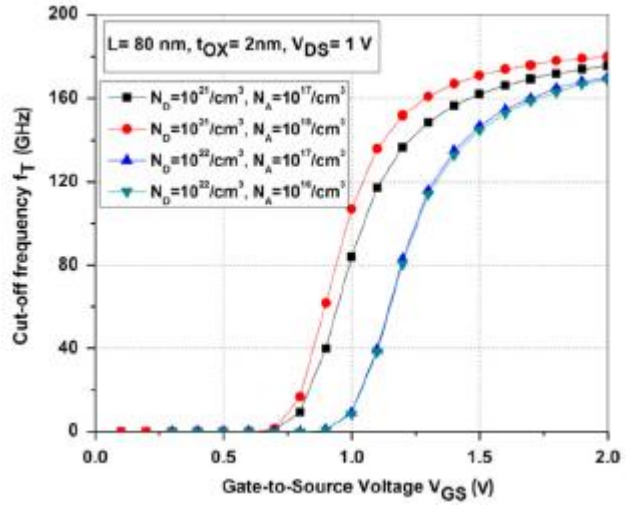

Figure 6. Unity-gain cut-off frequency (fT) as a function of gate-tosource voltage for various doping concentrations.

Variation of doping

The subthreshold swing, Ioff, and drain-induced barrier-lowering (DIBL) all improve significantly when the source-drain doping is lowered in the undoped channel experiment. Ion is the only trade-off. Reducing channel doping does not show a recognizable trend in improving device performance. However, when compared to a severely doped channel, it was discovered that the channel with no doping had a somewhat lower Drain-Induced Barrier Lowering (DIBL) and sub-threshold swing. When channel doping changes, device performance is primarily influenced by two things. One factor is the flat-band shift caused by channel doping, which reduces channel doping while increasing Ioff and VTh. As channel doping reduces, subthreshold performance improves and depletion thickness increases. In full-depleted silicon-on-insulator (SOI) devices, undoped channels are commonly used to reduce carrier surface scattering as channel thickness decreases. As the doping gradient of the source and drain extension (SDE) increases, so do the outer fringing and overlap capacitances, resulting in an overall increase in total gate capacitances. The resistance decreases significantly as the doping gradient intensifies. The intrinsic trade-off between resistance and parasitic capacitances necessitates an optimization.

Figures 6 and 7 show the relationship between gate-to-source voltage, maximum operating frequency (fMAX), and unity-gain cut-off frequency (fT) for different doping concentrations.

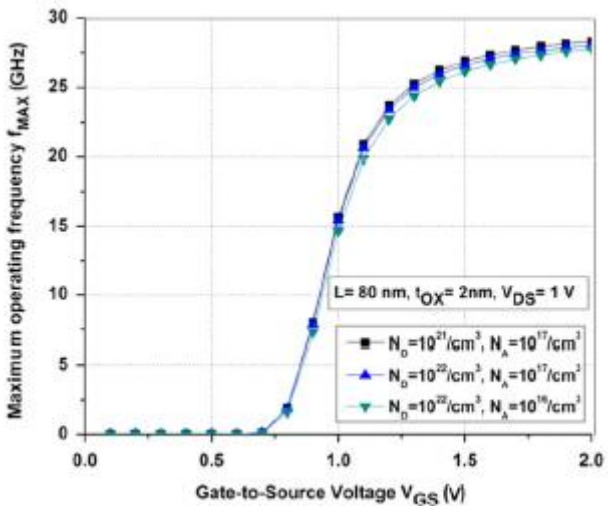

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Figure 7. Maximum operating frequency (fMAX) as a function of gate-to-source voltage for various doping concentrations.

Variation of overlap/underlap

The formula for the total effective gate capacitance is Cg eff = series(COX, CSi) || COV || Cif || [20]. The COV is determined by the channel width, oxide thickness, and overlap length in the Cof. Silicon capacitances are designated by the symbols CSi, Cif, and Cof, which stand for inner and outer fringe capacitance, respectively. Area per unit. Capacitance of Oxides Capacitance per unit area (COX) is calculated using the values of channel length (L), channel width (W), and oxide thickness (tox). The gate-to-source/drain overlap ensures the channel's electrostatic control, resulting in a strong Onstate current (Ion). However, the presence of high Miller capacitance degrades switching performance.

On the other side, an underlapped device can reduce undesirable overlap capacitance, but this reduces current drive and increases series resistance, leading in a lower SCE (subthreshold swing). However, when there is underlap on the source side, the influence of process fluctuations on the threshold voltage is exaggerated, resulting in a considerable decrease in ON current. Unlike double-gate (DG) MOSFETs, which benefit from a gate-underlap architecture, the results show that a gate-overlap construction is preferable in SNWTs [16, 21, 22]. As the overlap increases, the effective gate capacitance first increases before stabilizing. Internal peripheral capacitance Because of the overlap, the shorter the distance between the source/drain and the gate, the higher the Cif. Nonetheless, extreme inversion effectively shields the fringing field, resulting in the absence of Cif. The fringing capacitance (Cfr), which is a logarithmic function of the overlap, accounts for the majority of the overall gate capacitance (Cg) [23, 24]. As Ion and Ioff expand, their overlap increases, whereas gate overlap causes Cg to decrease. The increase in gate overlap predominantly reduces the effective channel length, resulting in an increase in drain current. When the overlap is large enough, the current grows linearly and becomes inversely proportional to the channel length. Regarding Supernova-Weighted Neutron Stars (SNWTs),

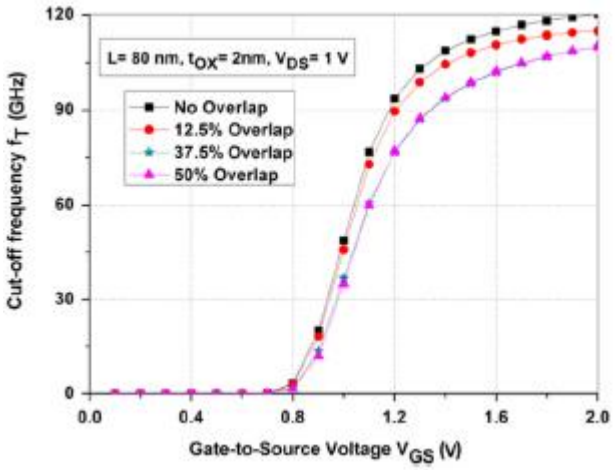

Figure 8. Unity-gain cut-off frequency fT as a function of gate-tosource voltage for gate underlap and overlap.

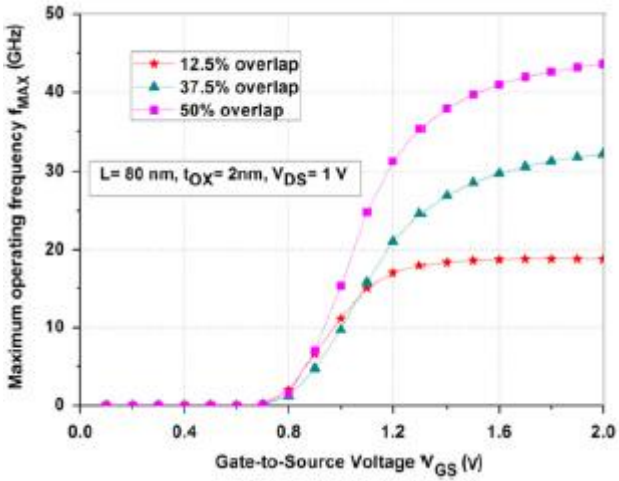

Figure 9. Maximum operating frequency fMAX as a function of gateto- source voltage for gate underlap and overlap.

These facts are most likely the fundamental cause of this. Initially, it appears that there are strict constraints for nanowire layout to reduce undesired resistance in the source-drain extension (SDE) areas. Parasitic capacitances in doping profiles are less affected by gradients if they are not large enough to cause considerable overlap capacitances. In contrast, DG MOSFETs have the outer-fringing capacitance as their primary source of parasitic capacitance. The effective

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management of SCE (short-channel effect) degradation is a critical aspect in the implementation of gate-underlap design for DG MOSFETs. Regarding SCE immunity, our simulation results show that gate-underlap design is unneeded for SNWTs because the GAA construction already provides adequate SCE effects.

Figures 8 and 9 show the relationship between gate-to-source voltage, unity-gain cut-off frequency (fT), and maximum operating frequency (fMAX) for gate underlap and overlap, respectively.

4. CONCLUSION

This study investigates the RF performance characteristics of a surrounding gate MOSFET, with an emphasis on several aspects such as oxide thickness (tOX), channel length (L), radius (R) of the cylindrical surrounding gate MOSFET, doping concentrations (Nd and Na), and gate geometry. Silvaco's ATLAS device simulator is used to examine the various figures of merit of RF performance parameters in a 2D scenario.

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