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# AN INTERLEAVED 6-LEVEL GAN BIDIRECTIONAL CONVERTER WITH AN ACTIVE ENERGY BUFFER FOR LEVEL II ELECTRIC VEHICLE CHARGING

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**ABSTRACT:**On-board electric vehicle (EV) devices have the capability of converting alternating current (ac) to direct current (dc), which can be used to power high-voltage battery packs. Because this sort of converter is permanently installed within a vehicle, it must exhibit excellent performance and power density. This is because the vehicle is designed to minimize power dissipation, system volume, and weight. An onboard charger must also provide bidirectional charging in order to allow auxiliary applications between the vehicle and the grid. This study describes the installation of a bidirectional single-phase alternating current-direct current converter capable of converting 400 $V_{DC}$ to universal alternating current (120-240 $V_{AC}$). The following are investigated: control, mechanical design and assembly, thermal management, and the interleaved 6-level floating capacitor multilevel (FCML) power factor correction (PFC) stage, as well as a twice-line-frequency seriesstacked buffer (SSB) stage. The experimental results demonstrate the operating mechanics of kilowatt-scale direct current to alternating current inverters. An study is conducted on a maximum power of 6.1 kW, and the results demonstrate that the efficiency exceeds 99%.

***Keywords:*** *Interleaved Converter,6-Level GaN (Gallium Nitride) Converter, Bidirectional Converter.*

## I. INTRODUCTION

To recharge an electric vehicle's (EV) high-voltage battery, Level II on-board adapters must be used, which are responsible for connecting to the alternating current (AC) grid. This makes it easier to operate a widely distributed infrastructure with power capacity in the kilowatt range and single-phase alternating current grid voltages (120-240 VAC). Given the restricted space and range capacities of electric vehicles (EVs), there is a considerable market need for tiny, lightweight, and highly efficient electric vehicle designs. The charger is constantly kept nearby, which is why this happens. The primary goal of this research project is to maximize the power density of a level II electric car charger's single-phase ac-dc stage while also considering converter topology, mechanical design and assembly, and thermal management into account. This will be

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performed within the scope of this research project. To achieve best performance, volumetric and gravimetric power densities are prioritized.

In order to create an alternating current to direct current stage in a typical architecture, a boost converter and a large bank of electrolytic capacitors are commonly used. By changing the current flow via the boost inductor, it is feasible to achieve accurate alternating current (AC) regulation while avoiding distortion and maximizing power factor outcomes. In applications involving single-phase alternating current-direct current (ac-dc) and direct current-alternating current (dc-ac), the capacitor bank is utilized to buffer power that pulses at double the line frequency. First and foremost, the boost inductor and electrolytic capacitor bank contribute significantly to the volume and bulk of these systems. Using specific designs, it is feasible to create a dc-ac stage by using the same circuitry in reverse mode.

The system's design incorporates a flying-capacitor multilevel (FCML) converter, which generates a rectified sine waveform or corrects the power factor (PFC), and a series-stacked buffer (SSB), which serves as the energy storage stage. This is done to optimize power density in terms of volume and weight. According to research, implementing the floating capacitor multilevel (FCML) design in inverter and power factor correction (PFC) applications significantly reduces the dimensions and mass of passive components. The assembly was designed using a modular and low-profile method, allowing for the most efficient use of three-dimensional space for mechanical packing. Automobile cooling systems are constructed with heat-generating components on a single side to obtain the best possible level of thermal efficiency through the use of direct circuit tracing.

This paper covers numerous aspects, including system architecture, thermal design, hardware and control, and packaging. At kilowatt power levels, the bidirectional design and control system stated in the previous research was able to successfully shift 400 VDC to 240 VAC, as evidenced by the test results. The remaining portions of the document are structured as follows: Sections II and III are devoted to exploring matters related to the system's design and architecture. Section V presents the results of the empirical research, Section VI presents the conclusions, and Section IV describes the physical hardware prototype.

## II. SYSTEM ARCHITECTURE

Figure 1 provides a complete illustration of the system's electrical schematic. The system consists of three components: an active rectifier/unfolder, an interleaved FCML PFC/inverter stage, and a series-stacked buffer. The buffer joins the ac and dc sides of the dc bus. Figure 2 shows a thorough control diagram displaying the SSB and inverter functions.

### A. FCML Stage

In the PFC/inverter stage, two FCML boost converters are interleaved. These converters maintain synchronization between the input voltage and the input AC current. In the context of the system operating

as an inverter, the rectified sine wave created by the FCML stage is transferred via the unfolder, rectified by the inductors, and completed by the system. The FCML architecture reduces inductor size by a factor of (N − 1)2 when compared to traditional two-level converters due to frequency multiplication. "N" signifies the total number of levels. A reduction in the inductor's size has resulted in improved power factor correction (PFC) performance.

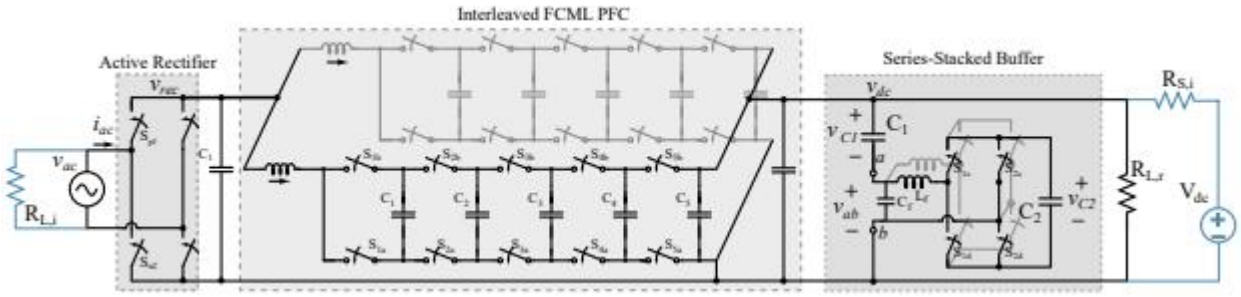


Fig. 1: Schematic of the overall system with active rectifier (unfolder), interleaved FCML PFC, and series-stacked buffer

The increased demand for control bandwidth complicates control and brings new issues. As previously explained, the problem with PFC control can be handled by incorporating a feed-forward term. To complete the final high-power test for this inquiry, the inverter mode control shown in Figure 2 is being used.

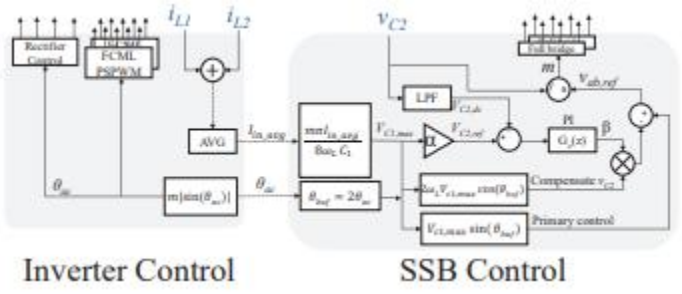


Fig. 2: Overall control system in inverter mode.

**B. Series-Stacked Buffer**

Figure 1 depicts a schematic depiction of the SSB. In a series configuration, a complete H-bridge converter is connected to the primary capacitor C1, which processes and stores energy. The full-bridge converter effectively reduces voltage ripple on VC1 by generating a waveform at vab that cancels out the ripple across the voltage. Using this strategy, the voltage variability on VC1 is exaggerated, resulting in a reduction in C1's required capacity by the same factor as the voltage variation. This is now possible because the direct current (dc) bus may be modified to ensure minimal fluctuation. Furthermore, the full-bridge converter operates at a lower voltage and contributes just a small percentage of the system's overall power. As a result, the entire voltage of the direct current (dc) bus is distributed over capacitor C1, boosting the system's efficiency. A feedback loop is a critical component in the formation of the canceling waveform vab; its primary function is to adjust the voltage VC2. As a result, while in operation, the SSB continues to take

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power from the full-bridge converter. As a result, the voltage on the direct current (DC) bus ripples, preventing the voltage drop on capacitor C2 caused by the full-bridge converter's losses. The overall SSB architecture has been established, including operational processes and large-scale deployment. To synchronize the phase and power relationships between the two stages, a control system is designed that combines PFC/inverter control and the SSB controller. This procedure is taken to ensure the desired alignment. During direct current (PFC) operation, the SSB controller is given two inputs: the angle of the AC voltage and the voltage-loop factor k, which is utilized to scale the input current. Using these recordings, one may estimate the stage and amplitude of the reference voltage for vab. Should you use an inverter?

This is performed by calculating the magnitude of vab using the average inductor current, as illustrated in Figure 2. To calculate the voltage vab for an alternating current (AC) with a sinusoidal waveform Vac sin (ωLt), use the following steps:

$$v_{ab} = \frac{P_0}{2\omega_L V_{dc} C_1} \sin(2\omega_L t),$$

The variable Vdc represents the average voltage of the direct current bus, whereas ωL represents the line's angular frequency. The power denoted as P0 represents the power utilized by the load. A detailed explanation of the hardware and software used to detect and regulate the PFC and inverter modes is made accessible.

## III. THERMAL DESIGN

To make the best use of the liquid cooling loops already installed in automobiles, a liquid cooling solution should be used to manage the heat generated by the electrical system components. A cool metal plate is used for heat dissipation. This plate is used to remove heat and is made up of 50/50 water and ethylene glycol (WEG). Heat is mostly generated by the inductors, which can each give up to 7.5 W of power, as well as the GaN devices, which can generate up to 5 W of power apiece. The smart plate was developed based on ANSYS IcePAK simulations of thermofluidic computational fluid dynamics (CFD). The integration of analytical models and simulations permitted quick iteration, finally leading to convergence on a design that effectively reduces pressure drop while providing suitable cooling for power electronic components. As shown in Figure 3, the channel layout, with a diameter of 0.125 inches, efficiently directs the majority of the fluid to the components with the maximum power density. To reduce the temperature difference between the frigid and other plates, a larger number of channels were developed and created. The cold plate layout was purposefully engineered to reduce thermal resistances and allow for efficient thermal contact while connected to the electric vehicle charger. This accomplishment was made possible by careful consideration of the various heights involved.

The computational examination of the cold plate was carried out using the ANSYS IcePAK domain, which has more than ten million cells. A mesh independence analysis was performed to see if the choice of finer

meshes had a significant impact on the results. This analysis was used to determine the chosen value. The steady-state simulations use a turbulent solver to reduce residuals to less than 10−6. The fluid input temperature for the automotive's cooling loop was defined to be 70 degrees Celsius, the maximum available temperature. As the electronic device's flow rate climbed to 1.1 LPM, the pressure difference between the intake and outflow dropped by 12.5 mbar. The electronic components' temperature increased significantly above the original temperature, reaching over 20 degrees Celsius. The ANSYS IcePAK simulations produced the data shown in Figure 5, which displays fluctuations in the electronics' maximum temperature and pressure drop between the intake and exit. The fluctuations are caused by changes in the rate of liquid movement. A flow rate increase from 1.1 to 5 LPM reduces the peak temperature by 4.5 degrees Celsius, resulting in a twenty-four-fold increase in the pressure drop across the system.

The 6063 aluminum alloy was chosen for the manufacture of the required cold plate because of its outstanding heat conductivity and light weight. The planned cold plate weighs 300 ± 0.5 grams and has a capacity of 0.17 ± 0.01 liters. Figure 4 depicts the following processes used in its development:

- Rough milling is used to remove large amounts of material and create height variations, as well as to create the cylindrical inlet and exit.
- A finishing pass is used to remove the final few millimeters of irregularity.
- Drilling is used to construct the inlet/outlet and interior channels.
- To seal the edge openings, use press-fitted epoxy to close the holes. The only unobstructed openings are the inlet and outflow.

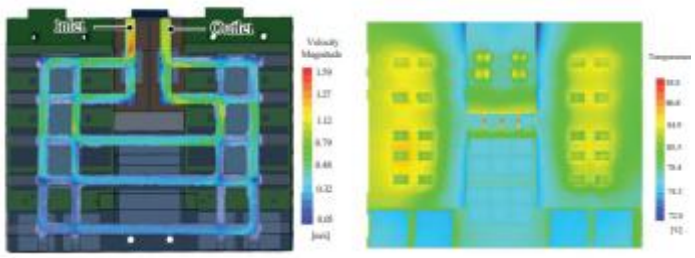

Fig. 3: The velocity magnitude contour plots and temperature estimates of the ANSYS IcePAK simulation of a 1.1 LPM flow inside the designed cold plate superimposed over the EV charger.

Fig. 4: The manufactured cold plate.

ISSN: 2366-1313

## IV. HARDWARE IMPLEMENTATION

The prototype merged mechanical, electrical, and thermodynamic design components in an efficient and harmonic manner. The FCML structure's versatility, which included mechanical and thermal arrangements, aided in the successful completion of the electrical design. Furthermore, the mechanical design optimizes the use of three-dimensional space to allow for the compact placement of components. Thermal management was required to employ a single-sided chilled design in order to optimize thermal circuit routing. The thermal management's goal was to steer the mechanical and electrical components toward a unified configuration in this design..

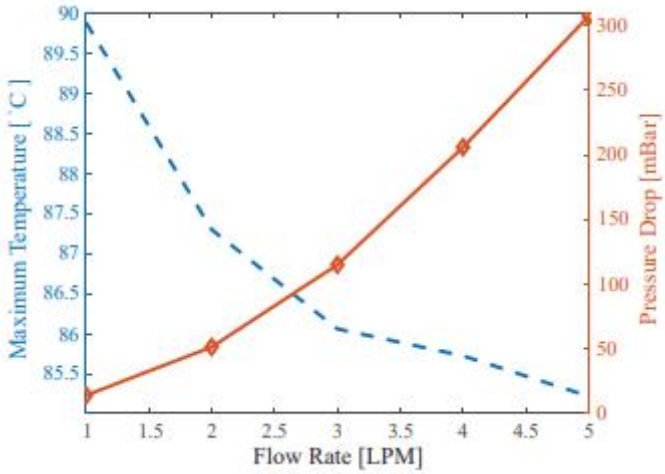


Fig. 5: ANSYS IcePAK simulation results of the maximum electronics temperature and the inlet-to-outlet pressure drop vs. the flow rate inside the designed cold plate.

TABLE I: Data Acquisition and Thermal Management Equipment

| Equipment | Description | Part Number |
|---|---|---|
| Chiller | Thermo Scientific Polar Series Accel 500 | 223422800 |
| Flow meter | Kobold MIM Series Electromagnetic Flow Meter | MIM-1215HG5C3T0 |
| RTDs | REOTEMP RTDs | AT-PX1123YLR4S1T2T |
| Data Acquisition Chasis | NI cDAQ-9189 CompactDAQ Chassis | 785065-01 |
| Analog Data Module | NI 9201 | 779013-01 |
| RTD Data Module | NI 9216 | 785186-01 |

Figure 6 depicts the building of a hardware prototype representing the intended architecture and control. The creation of this prototype has begun. A schematic illustration of a modular FCML converter (shown in Figure 7) was created to help expedite the production and investigation processes. The hardware prototype includes an H-bridge rectifier/unfolder, energy buffering capacitors, a series-stacked buffer twiceline frequency buffer stage, and two interleaved FCML converters. The operational converter was controlled by a TI C2000 microcontroller connected to it via a signal backplane board. Bolt-based connections are used to facilitate energy distribution amongst the main power circuits. Figure 8 is an exploded schematic that

ISSN: 2366-1313

provides a full visual overview of the prototype's electrical components. Figure 4 depicts the temperature management system's modified cold plate configuration. Refer to Section III for information on this design. Figure 9 depicts the experimental configuration, which includes the liquid chilling system and the temperature monitoring apparatus. Table I describes the apparatus used to collect data and identify problems with the liquid cooling system.

Each switch in the FCML stage must have a blocking voltage of 80 V (Vdc/5), which is equivalent to a maximum direct current of 400 VDC. As a result, GaN devices manufactured by GaN Systems and with a voltage rating of 100 V were chosen as the primary power sources. The GaN Systems devices, rated at 650 V, were inserted into the H-bridge unfolder stage to properly manage the 240 VAC line voltage. To meet the voltage requirements of the series-stacked buffer, which are 110 V, 150 V GaN devices manufactured by EPC Company are used as switches. Table II contains precise specs for the important components that make up the charger system.

## V. EXPERIMENTAL RESULTS

The high density implementation and control design were verified using the converter within the inverter.

TABLE II: Component listing

| Subsystem | Component | Part No. | Parameters |
|---|---|---|---|
| **Interleaved 6-Level FCML (per leg)** | GaN FETs | GaN Systems GS61008T | 100 V, 7 $m\Omega$ |
| | Isolated Gate Drivers | Si8271GB-IS | Silicon Labs Si827x Series |
| | Flying Capacitors | TDK C5750X6S225K250KA | 2.2 $\mu$F × 2–5 (parallel, ~ 2.6$\mu$F effective) |
| | Inductors | Vishay IHLP6767GZER100M11 | 10 $\mu$H |
| **Active Rectifier / Unfolder** | GaN FETs | GaN Systems GS66516T | 650 V, 25 $m\Omega$× 3 (parallel) |
| | Isolated Gate Drivers | Si8274GB1-IS1 | Silicon Labs Si827x Series |
| **Interleaved Series-Stacked Buffer (per leg)** | GaN FETs | EPC 2033 | 150 V, 7 $m\Omega$ |
| | Isolated Gate Drivers | Si8274GB1-IM1 | Silicon Labs Si827x Series |
| | Inductors | Coilcraft XAL7070-472 | 4.7 $\mu$H × 2 (series) |
| **Buffer Capacitors** | $C_1$ | TDK C5750X6S225K250KA | 820 (parallel) |
| | $C_2$ | TDK C5750X7S2A156M250KB | 200 (parallel) |
| **Control** | Microcontroller | TI F28379D controlCARD | C2000 Series Microcontroller |

ISSN: 2366-1313

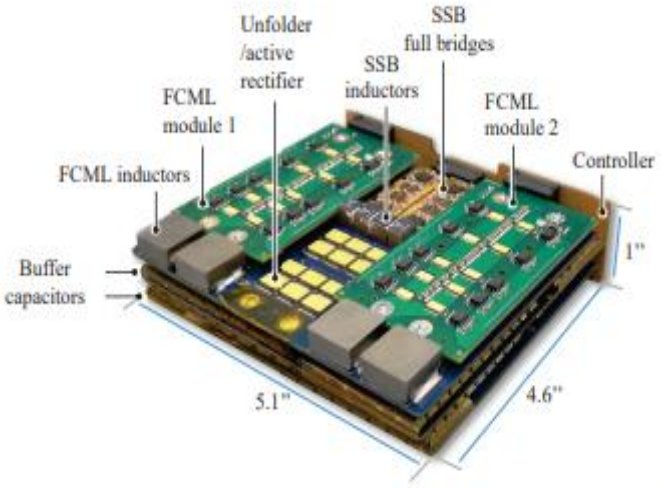


Fig. 6: The EV charger assembly, not including thermal management. Key subsystems are labeled.

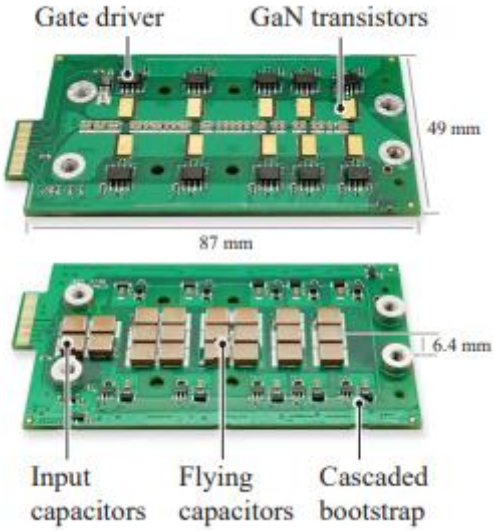


Fig. 7: Single FCML module with key components annotated.

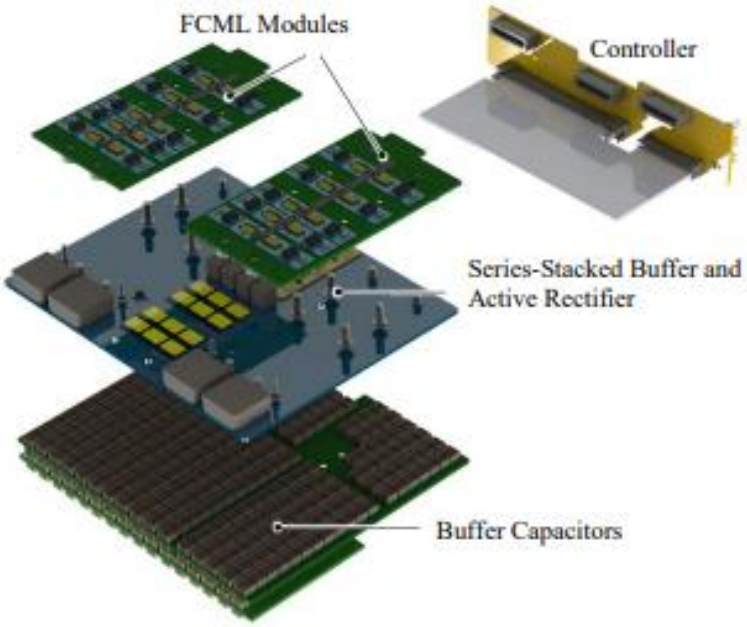

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Fig. 8: Exploded view render of the hardware assembly

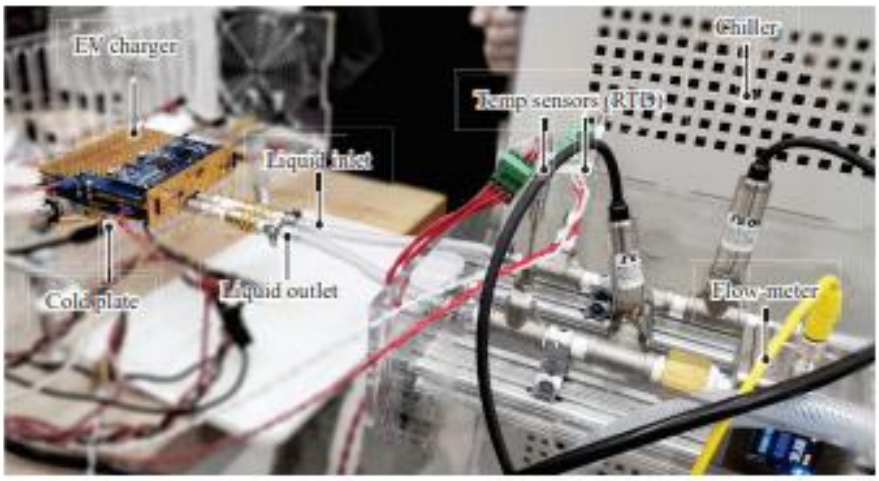


Fig. 9: Experimental bench setup.

Operating at maximum power. It was achieved by using a 400 VDC input voltage to generate a 240 VAC output. Extensive testing was carried out on the system while it was coupled to a cold plate system operating at 25 degrees Celsius. Figure 10 depicts the inverter stage's efficacy, including statistical data for input power up to 6.1 kW. The highest efficiency values, above 98.5%, occupy the majority of the spectrum and eventually exceed 99%. To attain extraordinarily high conversion efficiencies, a Keysight PA2201, a precision power analyzer, was used. Table III presents a thorough review of the converter's performance specifications. These characteristics include significant factors connected with power density and efficacy. Even without the cool plate, the system can generate 260 W/in3 of volumetric power density. When using the cold plate, however, the power density rises to 201 W/in3. Figure 11 depicts oscilloscope traces that serve as examples of typical converter waveform. The alternating current voltage is generated at the FCML's switch nodes (vsw1 and vsw2) using a filter. The SSB twice-line frequency buffering waveform (vab) is designed to eliminate the 120 Hz periodic oscillations that occur on the direct current (dc) buses. The vC2 waveform shows how the Single Sideband (SSB) feedback control ensures that the circuit branch receives sufficient real power to maintain the voltage on C2.

ISSN: 2366-1313

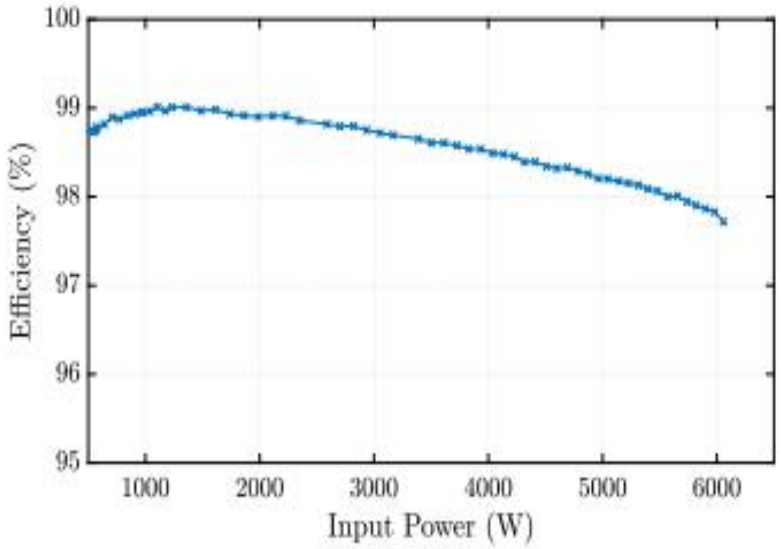


Fig. 10: The efficiency of the 6.1 kW inverter test, 400 $V_{DC}$ to 240 $V_{AC}$

TABLE III: Key Performance Specifications

| Parameter | Value | Notes |
|---|---|---|
| DC Voltage | 400 $V_{DC}$ | Tested |
| AC Voltage | 240 $V_{AC}$ | Tested |
| AC Current | 25 A | Tested |
| AC Power | 6.1 kW | Tested |
| Efficiency | 99.01% | Peak Eff. (At 1.1 kW) |
| | 97.7% | At 6.1 kW |
| Switching Frequency | 150 kHz | Per switch |
| Effective Frequency | 750 kHz | At inductor |
| Rect. Box Dimensions | 5.1" × 4.6" × 1.0" (12.95 cm × 11.68 cm × 2.54 cm) | Excl. cold plate |
| Cold plate Dimensions | 5.1" × 3.6" × 0.375" (12.95 cm × 9.14 cm × 0.95 cm) | |
| Volumetric Power Density | 260 W/in$^3$ (15.9 W/cm$^3$) | Excl. cold plate |
| Volumetric Power Density | 201 W/in$^3$ (12.3 W/cm$^3$) | Incl. cold plate |

ISSN: 2366-1313

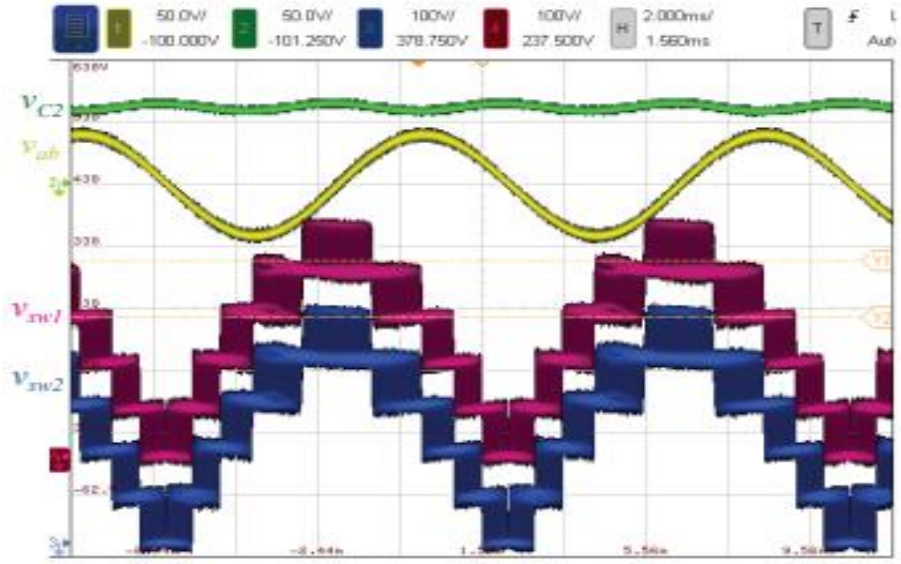


Fig. 11: Typical SSB voltage waveforms for $v_{c2}$ and $v_{ab}$, and FCML switching node voltages from 400 $V_{DC}$ to 240 $V_{AC}$, 6.1 kW.

## VI. CONCLUSION

This study aims to offer a Level II single-phase charging system for electric vehicles (EVs). The system has a series-stacked buffer structure as well as an interleaved flying capacitor multilevel converter (FCML) stage. The charger modulates its voltage by switching between 400 VDC and 120-240 VAC for the global AC voltage. This page provides a detailed explanation of the steps involved in developing the system's mechanical assembly, digital control, thermal management, and general architecture. By creating a hardware prototype, the operational capabilities of a dc-ac inverter capable of converting 400 VDC to 240 VAC were demonstrated. This prototype's construction is based on the demonstration of the PFC and inverter. The architecture and control architecture are discussed in [10]. When the power output is tested at its maximum of 6.1 kilowatts, the efficiency exceeds 99%.

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