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A FIVE-LEVEL INVERTER SINGLE SOURCE WITH A LOWER SWITCH COUNT

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ABSTRACT: A PWM control scheme for a dual reference single carrier single phase five-level inverter is provided. From the dc supply voltage, the inverter can provide five separate output voltage levels: Vdc, Vdc/2, 0, Vdc/2, and Vdc. To accomplish this, the suggested multilayer inverter requires an H-bridge cell, a bidirectional switch composed of four diodes and a switch, and a single DC voltage source coupled in series with two capacitors. When compared to conventional circuitry, the proposed solution reduces the number of switches and separate dc voltage sources.

Keywords: *Multilevel Inverter (MLI), Pulse Width Modulation, Total Harmonic Distortion (THD).*

1.INTRODUCTION

Multilevel inverter technology has lately emerged as a viable choice for medium-voltage, high-power applications. Researchers are still exploring for ways to apply optimal control methods to reduce the number of parts required and the cost of manufacture while maximizing their capabilities. The multilayer inverter has many applications, including power conditioning devices, motor drives, and the generation and distribution of renewable energy. PWM inverters can alter both the output voltage and frequency simultaneously. Furthermore, they can reduce the number of harmonics in the output current, improving total harmonic distortion (THD).

There have been numerous multilayer topologies proposed, but as output voltage levels increase, sdo switching strains, losses, and voltage imbalances between capacitors, among other problems.

Half and full bridge inverters require large input and output filters, a lower working voltage, significant harmonic distortion, and high electromagnetic interference (EMI) to function. MLI topologies are classified into three types: diode clamped, flying capacitor, and H-bridge converters with distinct DC sources. As the number of levels increases, more diodes are required for diode clamped MLI. To maintain volts stable, the flying capacitor MLI employs a massive number of capacitors. The only components required for a cascaded H bridge MLI are independent dc power sources for each H bridge. Using cascaded H-bridge multilevel inverters (CHBs) is one of the greatest techniques to increase the output voltage levels of standard multilevel inverters. The CHB includes extra switches, independent dc input voltage sources, and H-bridge cells. Using asymmetrical dc power sources is one technique to reduce the number of pieces in the CHB. The fundamental issue with the asymmetric cascaded H-bridge inverter is that it requires asymmetric DC sources to function.Proper separation can be achieved by employing a H Bridge with Multiple Transformer to reduce the number of switches.It also connects asymmetrical voltage sources to generate multiple output voltages. This approach makes use of a single source of DC power. However, it necessitates the use of two low frequency transformers, which increases the size and cost of the system. The capacitor serves as a DC power source in the case of a CHB with a single voltage source. The charging and draining of the capacitor

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must be closely monitored for this process to work. The modular multilayer converter was released. It's rather simple to add more levels, however there are more large capacitors and switches as the levels increase. Because they require fewer distinct DC sources, series connected capacitors are employed for the majority of popular procedures.

PWM is classified into three types: Space Vector PWM (SVPWM), Selective Harmonic Elimination PWM (SHEPWM), and Sinusoidal PWM (SPWM). SPWM is the most commonly utilized of them. Multi-carrier PWM and multi-reference PWM are the two types. There are two types of many-carrier PWM methods: phase-shifted and level-shifted. Level-shifted PWM systems are classified into three types: Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM, and Alternate Phase Opposition Disposition PWM. Multi-reference single carrier SPWM is superior to multi-carrier single reference SPWM in this scenario because it reduces the THD content of the output voltage [6]. This investigation demonstrates how to construct a five-level transformer using a single source and fewer parts. When a dual reference single carrier PWM technique is applied, the THD of the output voltage decreases. Computer-aided simulations in MATLAB/SIMULINK are used to ensure that the suggested method would work.

2.PROPOSED FIVE LEVEL PWM INVERTER CIRCUIT CONFIGURATION

The five-level inverter mentioned earlier is depicted below. It has an additional circuit, two capacitors connected in series, and a standard H bridge circuit. People believe that every component is flawless. Every capacitor has a voltage of Vdc/2 across it. As a result, the five output voltage values are Vdc, Vdc/2, 0, -Vdc/2, and -Vdc. The output voltage levels Vdc and -Vdc are provided by the H bridge cell. The extra circuit provides the other levels.

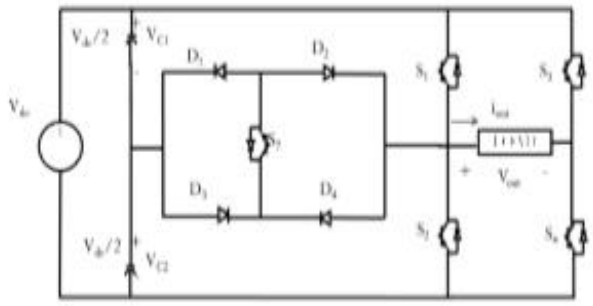

Fig. 1. A diagram of the previously mentioned five-level PWM inverter circuit.

3.GENERATION OF OUTPUT LEVELS

The five required output voltage values are generated by the following:

Vdc Level: When the switch is turned on, S2 connects the positive terminal of the load to Vdc, and S5 connects the negative terminal of the load to ground. Vdc is the voltage applied to the load lines when all other switches are turned off. The present pathways are depicted in Fig. 2 at this moment.

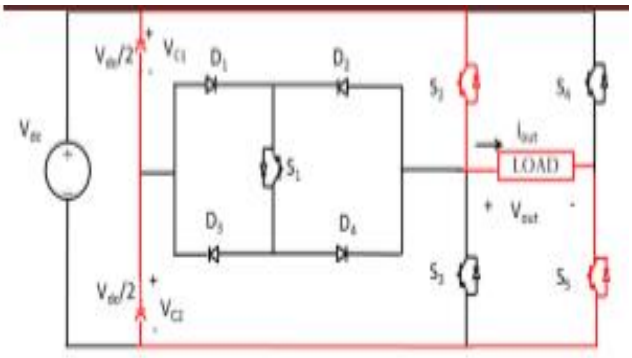

Fig.2. Configuring the Vdc voltage level and load current path

Vdc/2 level: 2.The load wires are connected to 2V, the auxiliary switch, S1, and S5 are all turned on, and all other controlled switches are turned off. The present pathways are depicted in Fig. 3 at this stage.

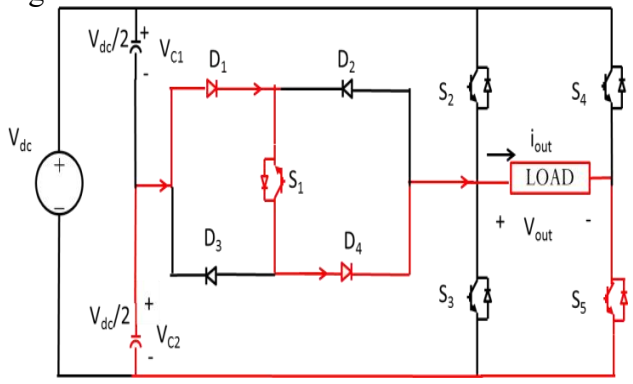

Fig.3. preparing the load current and the Vdc/2 voltage level.

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Because the load is short-circuited, there is no output because both main switches (S3 and S5) are turned on. The load terminals are not powered, and all other controlled switches are turned off. The present pathways are depicted in Fig. 4 at this point.

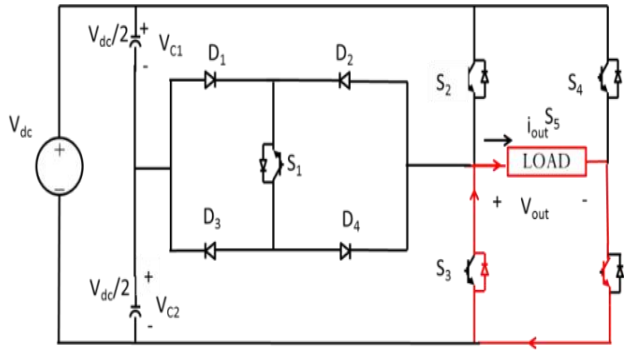

Fig.4. establishing a load current path and a zero voltage level

Vdc/2, negative output at half-level: The load terminals are connected to -Vdc/2, and the other controlled switches are turned off. S1 and S4 secondary switches are turned on. The present pathways are depicted in Fig. 5 at this stage.

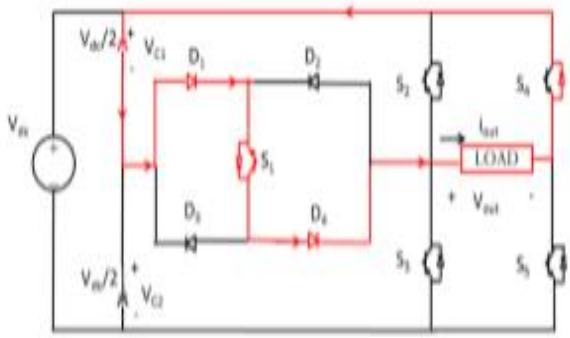

Fig.5. Generation of -*Vdc/2*voltage level and load current pat Figure 5 depicts the load current flow and voltage level at -2Vdc.

The load terminals are connected to -Vdc, S4 and S3 are both turned on, and all other regulated switches are turned off. Figure 6 depicts the present pathways at this time.

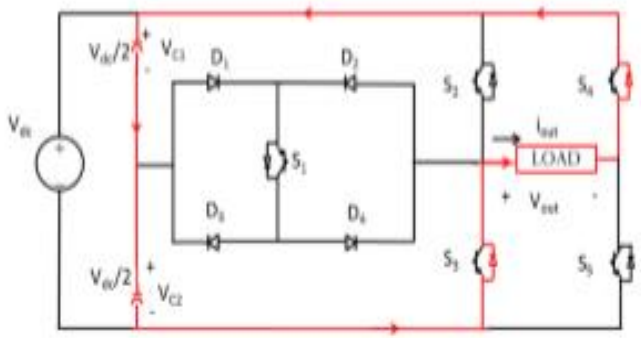

Fig.6. Creating a path for the load current and -Vdc voltage level

4.CONTROL SCHEME

The switching signals are generated using a single carrier multi reference PWM technique. A five-level inverter requires four high frequency carrier signals and one reference signal to perform multi-carrier SPWM. To create a five-level inverter, a multi-reference single carrier SPWM requires two reference signals and one high frequency carrier signal. In this scenario, a carrier signal and both reference signals are compared. They had the same frequency and amplitude as the carrier signal and were in phase with it. The amplitude of the carrier signal was equal to the offset number. Each reference signal and the primary signal had a difference.

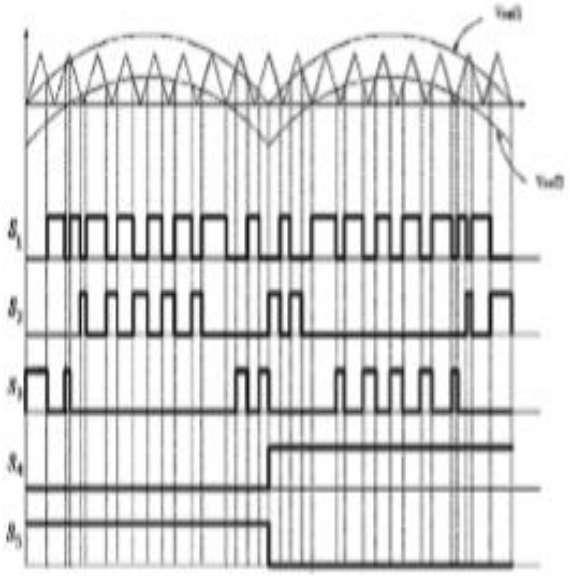

Fig.7. PWM is used in five steps to generate an alternating pattern of output voltage.

We will now compare the carrier signal to two reference signals, Vref1 and Vref2. If Vref1 is greater than Vcarrier, the peak level of the carrier signal, compare Vref2 to it until it equals zero. Vref1 now controls the comparison process until it defeats Vcarrier. The flipping pattern shown in Fig. 3 will then appear. S4 and S5 will operate at the same frequency as the fundamental frequency, however S1 through S3 will operate at the carrier frequency.

5.SIMULINK MODEL AND SIMULATION RESULTS

To ensure that the suggested inverter functioned, simulations were run in MATLAB/SIMULINK. The SIMULINK model for the five-level transformer is shown in Figure 8. The two

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capacitors divide the applied 100V input energy into two 50V pieces. The output voltage frequency is set to 50Hz.

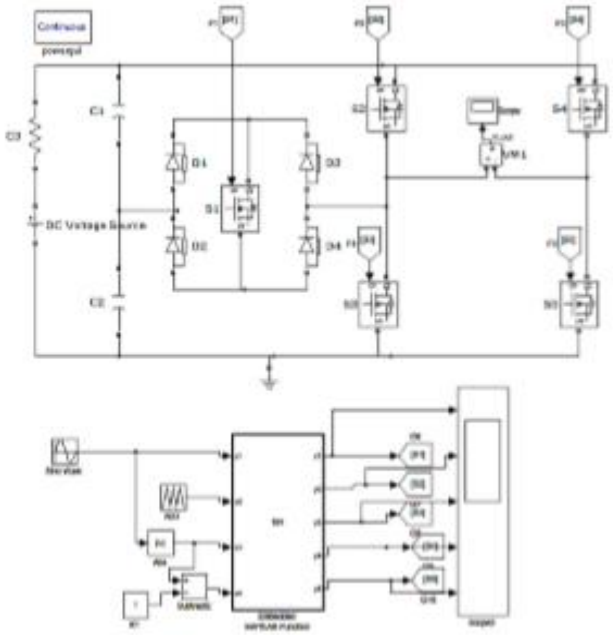

Fig.8. How the suggested system appears in Simulink

Figure 9 depicts the output voltage modeling results when the suggested switching approach is employed. The output voltage displays exactly five numbers.

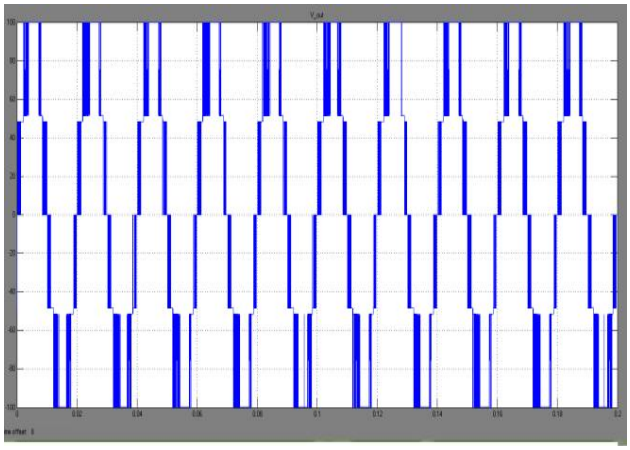

Fig.9. The suggested five-level inverter's output voltage

Figure 10 depicts how the THD of the output voltage is calculated and shown. THD is found to be lower than with typical topologies. Fewer parts are required to generate five output voltage levels than in usual configurations.

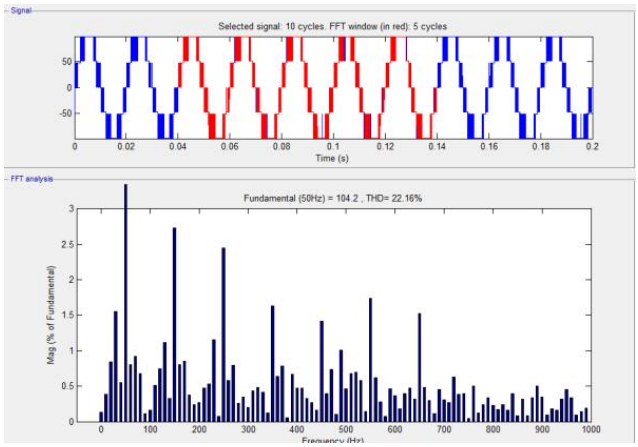

Fig.10. The suggested five-level inverter's output voltage

6.CONCLUSION

In this case, a multilayer PWM inverter is recommended. Using a single dc voltage source to enhance output voltage levels works well. The recommended multilevel inverter requires a single dc voltage source with two capacitors connected in series, an H-bridge cell, and a bidirectional switch made up of four diodes to function. Following a theoretical examination, computer simulations are utilized to ensure that the proposed method works. The described single source inverter has one source, fewer switches, and reduced switching stress. THD is reduced by the PWM control mechanism utilized here, which is dual reference single carrier sine PWM. In terms of power rating, the suggested 5-level PWM inverter can be an excellent alternative to ordinary PWM inverters for everyday use.

REFERENCES

1. Puyal. D, Barragan. L. A, Acero. J, Burdio.J. M and Millan. I, “An FPGA-based digital modulator for full or half-bridge inverter control,” IEEE Transactions on Power Electronics., 21(5), 1479–1483, Sept. 2006.
2. K.N.V.Prasad, G.R.Kumar, T.V.Kiran, G.S.Narayana, "Comparison of Different Topologies of Cascaded H-Bridge Multilevel Inverter", International Conference on Computer Communication and Informatics, January 2013.
3. Kui Wang, Yongdong Li, Zedong Zheng, Lie Xu, “Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter,”

ISSN: 2366-1313

IEEE Transactions on Industrial Electronics, vol. 60, no. 5, pp. 1943-1954, 2013.

4. Nasrudin A. Rahim, KrismadinataChaniago and JeyrajSelvaraj, "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System," IEEE Transactions on Industrial Electronics, Vol. 58, No. 6, June 2011.
5. YouheiHinago, Hirotaka Koizumi, "A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources," IEEETransactions on Industrial Electronics, vol. 57, no. 8, pp. 2643-2650, Aug. 2010.
6. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A Survey on Cascaded Multilevel Inverters", IEEE Transaction on Industrial Electronics, Vol. 1, No. 1December 2009.
7. K.Biju and R.Ramchand, "Modelling and Simulation of Single phase five level inverter fed from renewable energy sources",International Conference on Microelectronics, Communication and Renewable Energy,2013.
8. E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for gridconnected photovoltaic systems," IEEE Transactions on Industrial Electronics, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
9. Gerardo Ceglia, VíctorGuzmán, Carlos Sánchez, Fernando Ibáñez, Julio Walter, and María I. Giménez, "A New Simplified Multilevel Inverter Topology for DC–AC Conversion," IEEE Transactions on Power Electronics, Vol. 21, No. 5, September 2006.
10. N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Transactions Industrial Electronics, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.