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Error Detection and Correction code Techniques Development in Memory Applications

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Abstract: *Memory is a basic need in any SoC design. Memories are categorized into unpaired port memory and multiport memory. Multiport memory can perform more efficiently and overall high-speed performance compared to a single port. Semiconductor memory testing is increasing due to the high density of modern chips. Due to the increase in on-chip memory and memory density, the number of failures increases exponentially. Error detection works on the concept of redundancy, where more bits are added so that the real facts reach the error bits. Error correction is performed in two roles: one is that the receiver corrects the statistics, and the other is that the receiver sends the error bits back to the sender via feedback. The error can be detected and corrected in two ways. One is one bit, and the other is more than one bit. Single-bit error detection and correction are categorized into two parts, the classical algorithm, and the Mars algorithm. Subsequently, the second applied technique changed to extended broaching code (8, 4) or SECDED code ("single error correction - double error detection"). This code has one extra bit and is used for single error correction and double error detection. But double error correction does not appear in the S EC-DED code. Therefore, the SEC-DED (eight, four) code extension was SEC-DED-DAEC code (14,8) ("Single Error Correction – Double Error*

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Detection – Double Adjacent Error Correction"), where 14 stands for a generic code phrase, done Suggestion of 8 information bits and 6 parity bits that can be used for mismatch error correction and double error detection as well as double contiguous error correction in this work. Multi-bit error detection and correction are marked on adjacent symbols and random symbols. Various techniques are related to special types of errors that occur as errors.

***Keywords**: Multiple cell upsets, Error Detection and Correction codes, SRAM memories, Single Error Correction-Double Error Detection.*

I. INTRODUCTION

As there is a high demand for growth in capacitance, reduction in power, transistor dimensions, and working voltages, CMOS technology is shrinking. The demand for chip functionality has led to the growth of memory software. Embedded memory has been designed and used in a few sizes, around 14-16 nm, to meet the growing demand for chip storage capacity. Expanding the generation range and decreasing the conduction voltage can increase the sensitivity of memory cells to radiation elements. This problem occurs especially in memories. Many soft errors are caused by radiation, resulting in reliability issues [1].

Soft errors arise when neutrons are emitted from alpha debris from the wafer's coating fabric. The transients that act on the circuits corrupt the information stored in memories. When this single recording spoils a bit, it is called a slightly disappointing singleton; moreover, while more than one cell is damaged, it is defined as more than one motile problem. These simply spoil the stats but don't damage the entire device, which is why they are called soft bugs. Moreover, as the qubit cell density increases, many adjacent cells are also damaged, causing many multi-bit qubits and more of a mobile disorder. The main motive of this study is to detect those types of errors and also to identify these errors so that the transmission

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and reception events can be identified despite the possibility of noise interference across the channel [2].

The main objective of this research is to extend the SEC-DED code to the SEC-DED-DAEC code, and the pairwise errors detected are convergently corrected.

Memories are the most important theme included in the cute bugs. Embedded memory types, including ROM, SRAM, DRAM, and flash memory, are displayed across all machine chips. Memory failure costs are increasing due to generation scale, smaller dimensions, higher integration density, lower operating voltage, etc. A weak error occurs when a radiation event causes a rate disturbance sufficient to oppose or change the information state of a memory cell, register, latch, or flip. The error is "weak" because the circuit/tool is not permanently disabled with the help of radiation. If new data is written to the bit, the tool will effectively store it. Minor errors are also known as disappointment events. If the radioactive event is of very high strength, more than one bit will be affected, resulting in the development of a disappointing multiple bit instead of a single bit [3].

II. REVIEW OF LITERATURE

When the generation is reduced, code errors have been increased to reduce such error correction codes as the SEC-DED code with the help of using the mentioned green site and the algorithm, which is mainly based on the connection code that you can do randomly and exploit errors were used in the utility of the quantum system. Detection and debugging of various random and burst errors of a pair of bits are proposed in [4] using the diagonal hammer blade method. Suppose the spectrum detection and assignment are applied. In that case, the data transmission wants to be green, so the parity check hammer code is proposed along with the necessary coding and interpretation blocks. Because there are many errors, various codes have been proposed to debug redundant errors, such as matrix code based on hammer code and

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column line code, especially in the case of correcting memory errors in both information and parity down to a few bits entirely based on the 3D parity checking code proposed in [5]. Diagonal-horizontal-vertical methods have been proposed to detect and correct multiple-bit errors. The decimal matrix and equivalence codes were the error-correcting codes proposed to overcome the two cellular perturbations in [6]. Lightning-fast debugging codes have been suggested to reduce lag but with excessive redundancy. Error correction codes have been proposed to correct single and double adjacent errors. The SEC-DAEC code has been proposed. SEC-DED-DAEC code with enhanced decoding is suggested to reduce some mobile phone problems. SECDAED and SEC-DED-TAED codes are provided to detect modifications in memory designs. New codes have been introduced that provide basic SEC-DED and DAEC scalable error correction. Low complexity multi-bit error correction codes with low prices and excessive reliability have been proposed in [7]. The prices for soft errors will rise while the scope of generation occurs in memories, as quoted.

K. Rahul and S. Yachareni suggested that SRAM bit cells inside the IC could be accelerated after reducing technology. This will thrive within a wide variety of bidding errors. Here they used the SEC-DED code ("single error correction double error detection") and various strategies such as interleaving words and dragging columns if you want to reduce these errors. They also suggested green area codes (seventy-two, 64) and (39, 32) without adding more parity bits that can be used to detect adjacent three-bit errors and correct adjacent bit errors. Similarly, they suggested even the green (73,64) and (40,32) symbols with one extra parity if you want to identify and correct contiguous bit errors, 3-bit.

X. Zhong and G. Jin demonstrated a quantitative distribution software method. It is necessary to provide the quantum state of some other transient

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channel known as the quantum channel. However, due to some external factors, there is likely to be some exchange within the quantum world during transmission, which may cause errors in the physical key at the receiving end. A technique based on Hamming's code has been proposed and illustrated in this unique tool. This set of rules can be adapted to different bit error rates with the help of changing the coding duration. Furthermore, by incorporating the key interleaving algorithm, random and burst errors in the actual key can be corrected.

Subhasri. G and Radha. N proposed the detection and distribution of the spectrum are achieved because it may cause interference and errors in the original information. You want the data transfer method to be effective in troubleshooting and troubleshooting strategies. That was mainly implemented based on parity checking and code entry strategies. The encoder block was used to compute parity bits based primarily on the method's code for the input information. The decoder block was used to calculate the synchronization bit. These blocks were developed in the Xilinx Tool (ISE).

III. ERRORS DETECTION AND CORRECTION (EDC)

A. Error detection and correction

EDC is of two types. One is detecting and correcting a single error, and the other is detecting and correcting multiple errors. In an odd case, the EDC is used to find and select an error bit. These small errors can also be detected and corrected by some debugging code. The individual error codes are categorized into two types of algorithms. One is the traditional or traditional algorithm, and the other is the Mars algorithm. In some errors, detection and correction are of different types. For example, one is contiguous and different from a random one. Both have unique multi-bit detection and correction codes.

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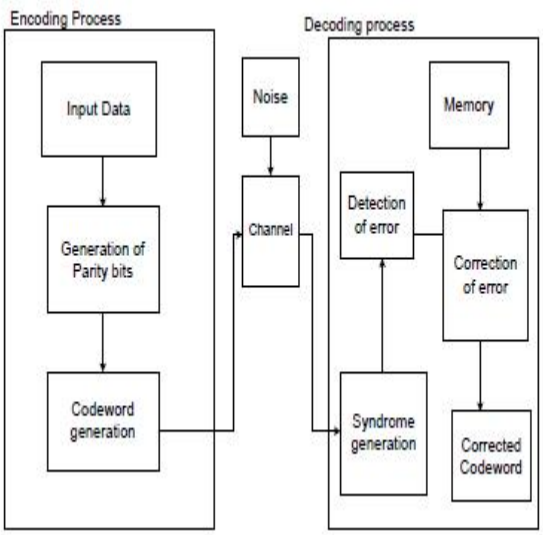

Fig.1 Block diagram for Error detection and Correction

B. Basic Coding Process

The error correction code A (d, b) has a d-bit word as input and a b-bit word as output. The input word d is a k-bit vector used to encode unique facts. And b is a vector of n bits, and (n – ok) are usually the trailing bits added to the input statement known as parity bits. When this b code phrase is transmitted through a channel, it produces the learned word. The error vector (e) is used to model the error that channel noise interferes with. If errors are not always present, then e is zero; In any other case, e is equal to at least one. The acquired statement is obtained with the help of XORing the symbol statement (b) and the error vector (e).

C. Hamming Code

These are linear correction symbols commonly used in memory and communication applications. These are used to detect and correct 1-bit errors with lower frequency. The code for methods (7, four) is given here. Where 7 stands for the generic code statement, four stands for the fact bits, and seven - four = 3 represents the parity bits that will be handed over to the stat bits. The drawback of this code is that it can only be used to detect and correct bit errors unrivalled. In this form of Hamming code encoding, there are 3 parity bits, P1, P2, P4, and 4 information bits, D1, D2, D3, and D4, and the total cipher body consists of seven bits which is a sequence of P1, P2, D1, P4, D2 bits, D3, D4. Equivalence expressions are given as follows,

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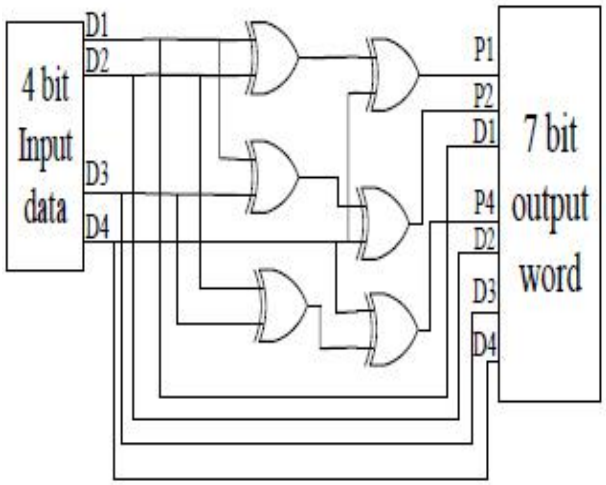

Fig 2: Hamming Code Encoder diagram

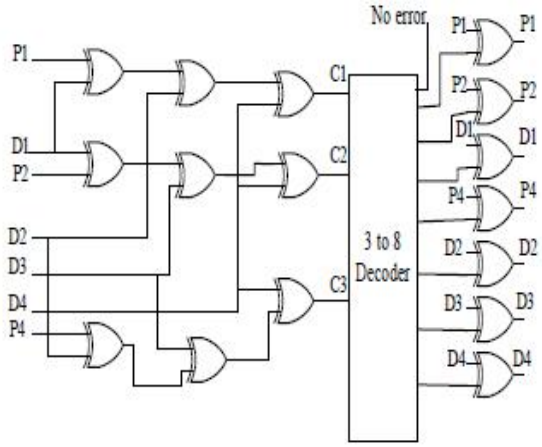

Fig.3 Hamming Code Decoder diagram

IV. SIMULATION RESULTS

All these Error Correction code techniques simulation results are verified by using Verilog Coding in Xilinx ISE 14.7 tool.

Hamming Code Encoder

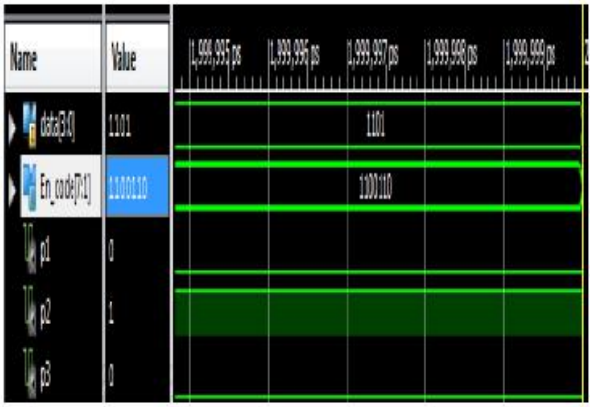

Fig.4 Hamming Code encoder output

Figure 4, the output encoding is obtained by combining 4 statistical bits and 3 parity bits. Here the input information data is obtained [3:0] = 1101 and p1, p2, p3 via the above parity expressions as a result of the output encoded [7:1] = 1100110

Hamming Code Decoder

In this Decoder process, there are 3 check bits c[0], c[1],c[2].

```
c[0]=En_code[1]^En_code[3]^En_code[5]^En_code[7]
c[1]=E_ncode[2]^En_code[3]^En_code[6]^En_code[7]
c[2]=En_code[4]^En_code[5]^En_code[6]^En_code[7]
```

In Figure 4, the acquired encoded output of Figure5 [7:1] = 1100110 with 1-bit errors in the first position is 1100111 and is provided as an input to the Hamming decoder, so 1-bit error detection and correction occurred. Output decoding result [7:1] = Output

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encoding [7:1] = 1100110. Therefore, the encoded output and decoded output are the same, so 1-bit error detection and debugging occurred with Hamming code.

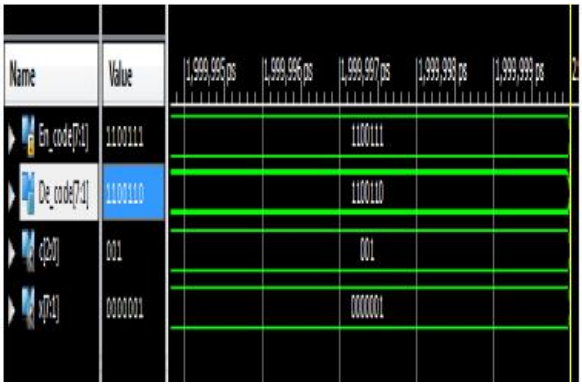

Fig.5 Hamming Code Decoder output for input=1100111

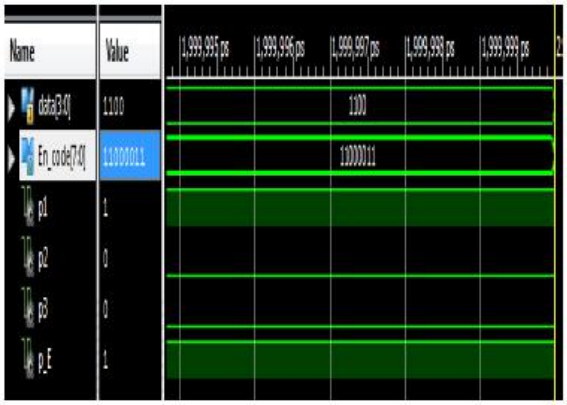

Fig.6 SEC-DED Code Encoder

In Figure 6, p_E = 1, this SEC-DED code is an extension of Hamming's (7,4) code, so the extra bit used for this code is calculated by XORing all data and parity bits. Here three parity bits, p1, p2, and p3, are calculated based on Hamming's symbol equations mentioned above. In this end result, p1 = 1, p2 = 0, p3 = zero and the input registers are [3:0] registers = 1100, the encoded output is a combination of all the information and parity bits, thus, encode[7:0] = 11000011

SEC-DED Code Decoder

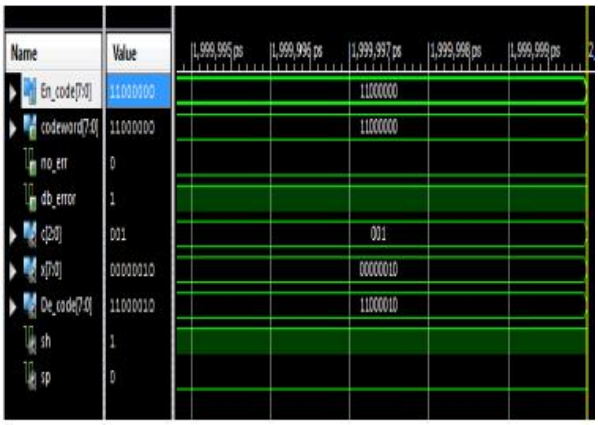

Fig.7 SEC-DED Decoder output when sh=1 and sp=0

In Figure 7, there are three test bits, c[0], c[1], and c[2], which can be fully computed based on Hamming code expressions. Based on the hammer symbol syndrome (sh) and valence syndrome (sp), specific operations are performed. When sh = 1 and sp = 0, double error detection takes a position where db = 1. When the encoded output = 11000011 is added with two errors in the two final positions, i.e.,

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11000000, and is given as input to the decoder, double error detection occurs db = 1. There is also an individual error correction.

V. CONCLUSION

As technology has shrunk, many soft errors have occurred in SRAMs, resulting in the single-cell configuration and more than one cell problem. Error-correcting codes, including the initial technique (7,4) hammer code where 7 denotes the generic code word, 4 denotes register bits, and 3 parity bits have been applied. Their coding and interpretation methods have been established. But it only became useful for detecting and correcting single-bit errors, which was the main drawback of this bridging code. Thus, the second method implemented became the elongated hammer code (8, four) or the SEC-DED code ("single error correction - double error detection"). This code has one extra bit and was used for single error correction and double error detection. But double error correction does not occur in the SEC-DED code. So the SEC-DED code extension (eight, 4) (14, eight) became the SEC-DEDDAEC code ("single error correction - double error detection - adjacent error correction") where 14 stands for the total code word, 8 information bits, suggested Six parity bits can be used for mismatch error correction and double error detection as well as adjacent double error correction in this work. These techniques associated with encryption and decoding methods were studied, and all simulation results were validated and executed using Verilog Coding on a Xilinx ISE 14.7 machine. The proposed SEC-DED-DAEC method was also implemented in-memory application and showed its performance. Side-by-side double-fault detection with this method is fixed, and complexity is reduced. The advantage of this proposed method was may be able to stumble on minute adjacent errors, and the dilemma becomes that there may be a spread of multiple errors, so this would be a similar range for this work. This work

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introduced error detection and correction up to 2 bits.

REFERENCES

1. *D.Vijaya Saradhi, K.Swetha, 2021, "Shielding performance analysis of flexible multi-layered textile sheets based on polymer substrate", Materials Today: Proceeding*
2. *Vijaya Saradhi Dommeti, Dharma Raj Cheruku, 2020, "Multi-layer composites shielding for electromagnetic radiation protection", Int. J. Advanced Intelligence Paradigms, DOI:10.1504/IJAIP.2020.108772,*
3. *Vijaya Saradhi Dommeti, 2020, "Vijaya Saradhi Dommeti, "Development of Laminated Electromagnetic Shield", LAP*
4. *C. D. Raj, D. V. Saradhi "Development of a multilayer conductor electromagnetic shield for optimum shielding performance", ICWET '11 International Conference & Workshop on Emerging Trends in Technology.*
5. *K. Rahul and S. Yachareni, "Area and power efficient ECC for multiple adjacent bit errors in SRAMs.," 2020 IEEE Internat ional Conference on Consumer Electronics (ICCE), Las Vegas, NV, USA, 2020, pp. 1-4, doi: 10.1109/ ICCE46568.2020.9042979.*
6. *X. Zhong and G. Jin, "Application of Hamming Code Based Error Correct ion Algorithm in Quantum Key Distribut ion System," 2020 IEEE 3rd Internat ional Conference on Elect ronics Technology (ICET), Chengdu, China, 2020, pp. 857-861, doi: 10.1109/ICET49382.2020.9119567.*
7. *G. M. Sai, K. M. Avinash, L. S. G. Naidu, M. S. Rohith and M. Vinodhini, "Diagonal Hamming Based Multi-Bit Error Detect ion and Correct ion Technique for Memories," 2020 Internat ional Conference on Communicat ion and Signal Processing (ICCSP), Chennai, India, 2020, pp. 0746-0750,doi: 10.1109/ICCSP48568.2020.9182249*
8. *Prasadu Peddi (2019), Data Pull out and facts unearthing in biological Databases, International Journal of Techno-Engineering, Vol. 11, issue 1, pp: 25-32.*
9. *J. Gracia-Morán, L. J. Saiz-Adalid, D. Gil-Tomás and P. J. Gil-Vicente, " Improving Error Correction Codes for Mult iple-Cell Upsets in Space Applicat ions," in IEEE Transact ions on Very Large Scale Integrat ion (VLSI) Systems, vol. 26, no. 10, pp. 2132-2142, Oct. 2018, doi: 10.1109/TVLSI.2018.2837220.*

ISSN: 2366-1313

10. *Prasadu Peddi (2019), "AN EFFICIENT ANALYSIS OF STOCKS DATA USING MapReduce", ISSN: 1320-0682, Vol 6, issue 1, pp:22-34.*